System-on-a-Chip, Gangable DPS/VI/PMU

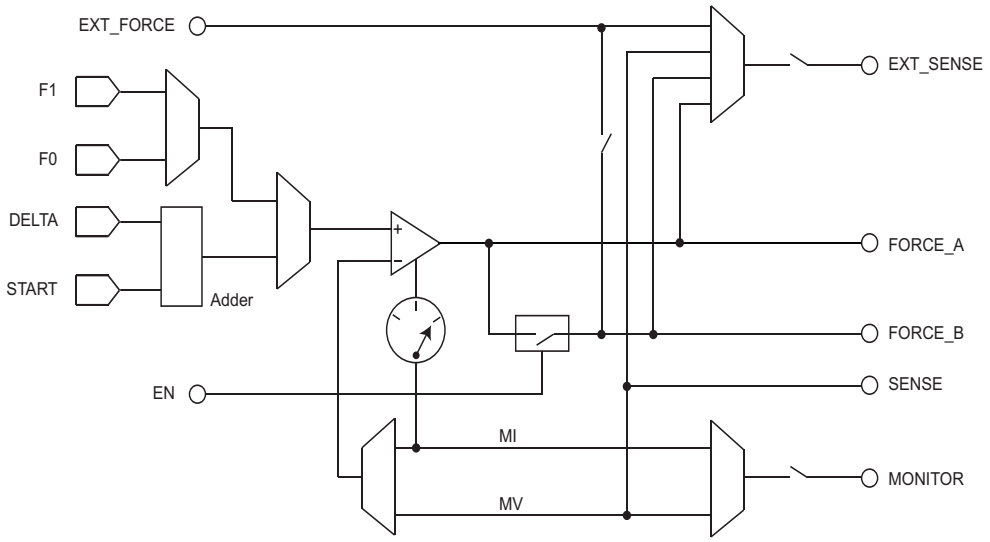
The Jupiter is a highly integrated System-on-a-Chip (SOC) Device Under Test Power Supply (DPS) incorporating all analog and digital functionality required for a single DPs unit for Automated Test Equipment. the interface, the control, and the I/O are digital. All analog circuitry is inside the chip. One chip constitutes one complete DPS.

Features

- 1A DC Output Drive Capability
  - 6 Current Ranges (1,024mA, 128mA, 8mA, 1mA, 125µA, 15.625µA)
  - Glitchless Current Range Changing
  - HiZ Capability w/Extremely Low Leakage
- Full Functionality
  - FV, FI, MV, MI
  - 4 Quadrant Operation
  - Bump Function
- Ganging Capability for Higher Current Applications
- Integrated External Force and Sense Switches
- Independent Power Supply for Output Stage
- Operating Voltage
  - 24V Supply Range
  - Adjustable Output Range
  - 4 Voltages Ranges (4V, 8V, 16V, 24V)
  - Adjustable Slew Rate
  - External Precision DAC Drive Capability
- Programmable Clamps
  - Voltage Clamps
  - Current Clamps
- Ultra Low Noise External DAC Mode
- Programmable Alarms
  - Over Current
  - Over Voltage
  - Over Temperature
  - Kelvin Sense
- Dedicated Real Time DAC for Forcing Level
  - Increment/Decrement Option
  - Linear/Binary Increment/Decrement Option
  - 16-bit per Level Offset and Gain Correction
- On-Chip DC Support Levels
  - 16 Bits per Level
  - 16 Bit per Level Offset and Gain Correction
- 3-Bit Serial CPU Port
  - Load Internal Registers and Memory
  - Read Back Internal States
- Package
  - Lead Free
  - 64 Lead, 10mm x 10mm TQFP with Heat Slug
- Power Dissipation
  - Pdq (No Load) = 700mW to 1.5W

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers



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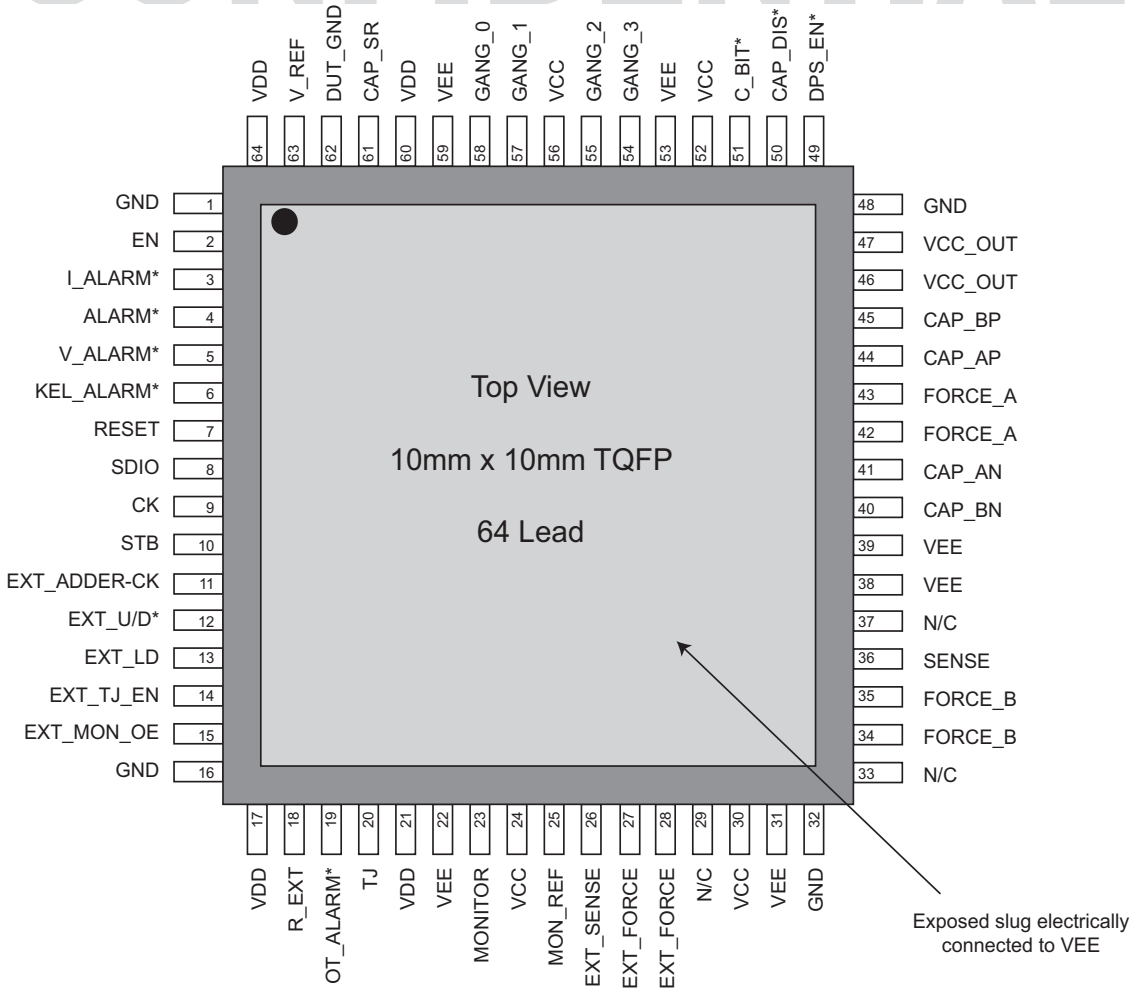
PIn Descriptions

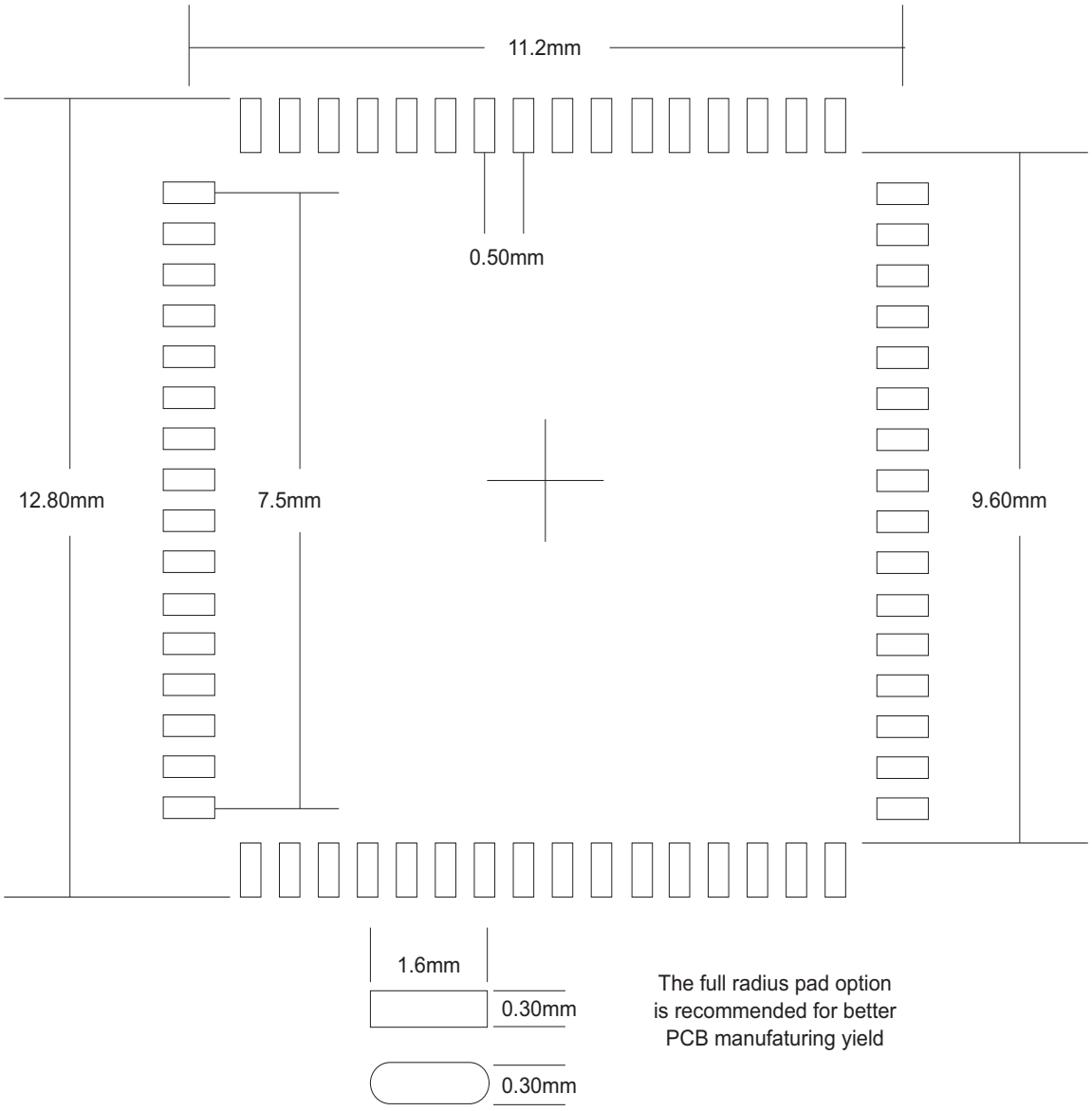
Pin Number	Pin Name	Description
Real Time Digital Inputs/Outputs		
2	EN	Real time digital input that turns the DPS on and off.
49	DPS-EN*	Open drain digital output used to control the off-chip HiZ switch.
50	CAP_DIS*	Open drain digital output used to disconnect the off-chip capacitor on FORCE.
51	C_BIT*	Open drain digital output for a spare control bit.
Alarms		
4	ALARM8	Open drain digital output indicating any alarm condition.
5	V-ALARM*	Open drain digital output indicating an over voltage flag.
3	I_ALARM*	Open drain digital output indicating an over current flag.
19	OT_ALARM*	Open drain digital output indicating an over temperature flag.
6	KEL_ALARM*	Open drain digital output indicating a Kelvin flag.
External Controls		
11	EXT_ADDER_CK	Digital input that updates the adder.
12, 13	EXT_U/D*, EXT_LD	Digital inputs that determine the adder mode.
15	EXT_MON_OE	Digital input that places the MONITOR in HiZ.
14	EXT_TJ_EN	Digital intput that controls the TJ output high impedance.
DUT Pins		
42, 43	FORCE_A	Output force pins without HiZ.
34, 35	FORCE_B	Output force pins with HiZ.
36	SENSE	Output sense pin.
High Voltage Analog Pins		
23	MONITOR	Analog voltage output that tracks the measured parameter.
25	MON_REF	Monitor reference voltage.
62	DUT_GND	Analog input voltage used to track GND at the DUT.
58, 57, 55, 54	GANG_0 - GANG_3	Analog input/output voltages used when ganging multiple DPS units.
27, 28	EXT_FORCE	External bypass pins that provide direct access to FORCE_B.
26	EXT_SENSE	External bypass pin that provides direct access to internal nodes.
44, 41	CAP_AP, CAP_AN	Pins for external compensation capacitors.
45, 40	CAP_BP, CAP_BN	Pins for external compensation capacitors.
61	CAP_SR	Pins for an external capacitor for slew rate adjust.
Low Voltage Analog Pins		
63	V_REF	External precision voltage reference.
18	R_EXT	External precision voltage reference.
20	TJ	Analog output voltage that corresponds to the function temperature.

CPU Interface		
9, 8, 10	CK, SDIO, STB	3-bit serial port (Clock, Data, Strobe).
7	RESET	Chip Reset
Power Supplies		
17, 21, 60, 64	VDD	Digital power supply.
24, 30, 52, 56	VCC	Positive analog supply.
46, 47	VCC_OUT	Positive analog supply for the output stage.
Miscellaneous		
22, 31, 38, 39, 53, 59	VEE	Negative analog supply.
1, 16, 32, 48	GND	Device ground.

Pin Configuration



Recommended PCB Footprint



Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supplies			
VCC	VDD – 0.4	+25	V
VEE	–20	+0.4	V
VDD	–0.4	+5	V
VCC – VEE	0	+25	V
VCC_OUT	0	VCC	V
Analog Force/Sense Pins			
FORCE_A, FORCE_B, SENSE	VEE – 0.7	VCC + 0.7	V
Output Currents			
SDIO	–20	20	mA
All ALARM* Outputs		20	mA
Control Pin Outputs			
C_BIT*, DPS_EN*, CAP_DIS*	GND – 0.7	VCC + 0.7	V
External References			
V_REF	GND – 0.25	VDD + 0.25	V
R_EXT	9	11	KΩ
EXT_SENSE, EXT_FORCE	VEE – 0.7	VCC + 0.7	V
MONITOR, GANG_<0:3>	VEE – 0.7	VCC + 0.7	V
Temperature			
Junction Temperature	–25	150	°C

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+6		+19	V
VCC_OUT	+6		VCC	V
VEE	–16		–5	V
VDD	+3.25	+3.3	+3.45	V
GND		0		V
VCC – VEE	+13		+24	V
VCC_OUT – VEE (500mA Load)		20		V
Digital Inputs/Outputs				
CK, SDIO, STB, RESET	GND		VDD	V
On-Chip DC Levels				
RT_DAC	VEE + 3		VCC – 3	V
V_CI-Hi, V-CI-Lo	VEE + 2		VCC – 2	V
V-CI-Hi – V_CI-Lo	+1			V
I-CI-Source, I-CI-Sink	0		+2	V
External References				
V_REF	+2.99	+3.0	+3.01	V
R_EXT	9.99	10.0	10.01	KΩ
DUT_GND	–1		+1	V
Analog Pins				
FORCE_B (active No Load)	VEE + 1		VCC_OUT – 0.5	V
FORCE_B (active No Load)	VEE + 1		VCC – 3	V
FORCE_B (active 500mA Load)	VEE + 3		VCC_OUT – 3	V
FORCE_B (active 500mA Load)	VEE + 3		VCC – 3	V
FORCE_B (in HiZ)	VEE		VCC	V
GANG_0 to GANG_3	VEE		VCC	V
TJ	GND		VDD	V
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
Monitor				
HiZ Compliance	VEE		VCC	V
Active	VEE + 2		VCC – 3	V
Operating Conditions				
Junction Temperature	25		100	°C
CPU Port Frequency	10		20	MHz
Maximum DUT Capacitance (FV Mode)			50	µF
Maximum DUT Capacitance in Bypass Mode			1	nF

Recommended Operating Conditions - cont'd

Parameter	Min	Typ	Max	Units
Maximum DUT Capacitance (FI Mode)				
IR0			1	µF
IR1			10	µF
IR2			50	µF
IR3			50	µF
IR4			50	µF
IR5			50	µF

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Characteristics - Power Supplies

.R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units	Pd (Typ)
Positive Shift, No Load							
11100	VCC	Iout = 0mA; V_FV = +5.0V; Note 1	20	30	40	mA	570mW
11400	VCC_OUT		1	5	9	mA	95mW
11200	VEE		22	32	42	mA	160mW
11300	VDD		13	20	27	mA	66mW
							891mW/Chip
Positive Shift, Sourcing 512mA							
11110	VCC	Iout = 512mA; V_FV = VCC – 10V; Note 1	20	30	40	mA	570mW
11410	VCC_OUT		512	540	575	mA	5,400mW
11210	VEE		45	55	65	mA	275mW
11310	VDD		13	20	27	mA	66mW
							5.3W/Chip
Positive Shift, Sinking 512mA							
11120	VCC	Iout = –512mA; V_FV = VEE + 10V; Note 1	35	45	55	mA	855mW
11420	VCC_OUT		12	20	28	mA	380mW
11220	VEE		550	575	600	mA	5,750mW
11320	VDD		13	20	27	mA	66mW
							7.0W/chip
Negative Shift, No Load							
11130	VCC	Iout = 0mA; V_FV = +5.0V; Note 2	20	30	40	mA	360mW
11430	VCC-OUT		1	5	9	mA	60mW
11230	VEE		22	32	42	mA	384mW
11330	VDD		13	20	27	mA	66mW
							870mW/cjhip
Low Voltage, No Load							
11140	VCC	Iout = 0mA; V_FV = +5.0V; Note 3	20	30	40	mA	450mW
11440	VCC_OUT		1	5	9	mA	40mW
11240	VEE		22	32	42	mA	256mW
11340	VDD		10	18	25	mA	59mW
							805mW/Chip

Notes:

1. VCC = +19.25V, VCC_OUT = +19.25V, VEE = –5.25V, VDD = +3.45V.
2. VCC = +12V, VCC_OUT = +12, VEE = –12V, VDD = +3.45V.
3. VCC = +14.75V, VCC_OUT = +7.75V, VEE = –7.75V, VDD = +3.25V.

DC Characteristics - CPU Port

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V

Spec #	Parameter	Conditions	Min	Typ	Max	Units
SDIO, CK, STB, RESET						
17100	VIH	Note 4	2.0			V
17110	VIL	Note 4			0.8	V
17120	Iin (Input Leakage Current)	Tested at 0V and VDD; Note 5	–100	0	+100	nA
17200	VOH (SDIO only)	Output Current = 8mA; Note 4	2.4			V
17210	VOL (SDIO only)	Input Current = 8mA; Note 4			0.8	V

DC Characteristics - Digital Inputs (EN, EXT_ADDER_CK, EXT_U/D*, EXT_LD, EXT_MON_OE, EXT_TJ_E

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V

Spec #	Parameter	Conditions	Min	Typ	Max	Units
13260	VIH	Note 4	2.0			V
13261	VIL	Note 4			0.8	V
13262	Iin (Input Leakage Current) (HiZ)	Tested at 0V and VDD; Note 5	–100	0	+100	nA

DC Characteristics - Digital Outputs

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
V_ALARM*, I_ALARM*, OT_ALARM*, KEL_ALARM*, ALARM*						
19117	VOL (sinking 8mA)	Note 4		0.1	0.4	V
13361	Pull-Up Resistance	Tested at 0V; Note 5	–40	52	64	KΩ
DPS_EN*, CAP_DIS*, C_BIT*						
19114	VOL (sinking 20mA)	Note 4		0.5	1.0	V
13461	IOH (HiZ Leakage)	Tested at 0V and VDD; Note 5	–100	0	+100	nA

NOTES:

4. VCC = +19V, VCC_OUT = +19V, VEE = –5V, VDD = +3.3V,
5. VCC = +19.25V, VCC_OUT = +19.25V, VEE = –5.25V, VDD = +45V,

DC Characteristics - Analog Pins

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
10999	V_REF Input Current	Tested at 0V and VDD; Notes 6, 7	–1	0	+1	µA
10998	DUT_GND Input Current	Tested at 0V and VDD; Note 6	–1	0	+1	µA
14090	FORCE_B HiZ Leakage	Tested at FORCE_B = 0V; Notes 6, 7	–25	0	+25	nA
14091	FORCE_B HiZ Leakage	Tested at FORCE_B = VCC – 2V; VEE + 2V; Notes 6, 7	–35	0	+35	nA
10997	High Leakage: SENSE, GANG_#, EXT_FORCE, EXT_SENSE	Tested at 0V; Notes 6, 7	–15	0	+15	nA
10996	High Leakage: SENSE, GANG_#, EXT_FORCE, EXT_SENSE	Tested at VCC – 2V and VEE + 2V; Notes 6, 7	–25	0	+25	nA
14095	High Leakage: CAP_SR, CAP_AP, CAP_AN, CAP_BP, CAP_BN	Tested at 0V; Tested at VCC – 2V and VEE + 2V; Notes 6, 7	–100	0	+100	nA

NOTES:
6. VCC = +19V, VCC_OUT = +19V, VEE = –5V, VDD = +3.3V,
7. VCC = +12V, VCC_OUT = +12V, VEE = –12V, VDD = +345V,

DC Characteristics - Static DAC Calibration

All DC tests are performed after the Static DAC is calibrated. The upper 5 bits of the Static DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carries as small as possible.

VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
16510	D15 Step Error	Code 8000 – Code 7FFF – LSB; VR1; Note 8	–5		+5	mV
16520	D14 Step Error	Code 4000 – Code 3FFF – LSB; VR1; Note 9	–5		+5	mV
16530	D13 Step Error	Code 6000 – Code 5FFF –LSB; VR1; Note 10	–5		+5	mV
16540	D12 Step Error	Code 7000 – Code 6FFF – LSB; VR1; Note 11	–5		+5	mV
16550	D11 Step Error	Code 7800 – Code 77FF – LSB ; VR1; Note 12	–5		+5	mV

NOTES:
8. (DAC @ B000 – DAC @ 3000) / (B000 –3000) – DAC LSB; VR1
9. (DAC @ 7000 – DAC @ 3000) / (7000 – 3000) – DAC LSB; VR1
10. (DAC @ 7000 – DAC @ 5000) / (7000 – 5000) – DAC LSB; VR1
11. (DAC @ 7000 – DAC @ 6000) / (7000 – 6000) – DAC LSB; VR1
12. (DAC @ 7800 – DAC @ 7000) / (7800 – 7000) – DAC LSB; VR1

DC Characteristics - Static DAC

There are 3 on-chip internal DACs per channel used for:

1. Static DAC Level
2. Static DAC Offset Correction
3. Static DAC Gain Correction

DAC testing is performed post Static DAC Calibration.

VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.. DAC tests performed using the PMU in FV mode and the MONITOR output VR1.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Level DAC Test						
16100	Span	Notes 13, 14	7.6	8.0	8.4	V
16110	Linearity	Notes 13, 15	–10	0	+10	mV
16120	Bit Test	Notes 13, 16	–10	0	+10	mV
16190	Droop Test	Note 20			300	µV/ms
16401	RMS DAC Noise Test				500	µV
Offset DAC Test						
16200	+Adjustment Range	Notes 17, 18	+5.2	+6.0	+6.6	% of Span
16210	–Adjustment Range	Notes 17, 18	–6.6	–6.0	–5.2	% of Span
16220	Linearity	Notes 15, 18	–10	0	+10	mV
16230	Bit Test	Notes 16, 18	–10	0	+10	mV
Gain DAC Test						
16300	+Adjustment Range	Note 19	1.07	1.125	1.15	V/V
16310	–Adjustment Range	Note 19	.850	.875	.922	V/V
16320	Linearity	Notes 15, 19	–2	0	+2	mV/V
16330	Bit Test	Notes 16, 19	–2	0	+2	mV/V

NOTES:

13. Offset and Gain DACs both programmed to midscale (Code 7FFF).
14. Span = DAC(FFFF) –DAC(0000),
15. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF.
16. Bit Test - Walking 1 and Walking 0 to determine the correct bit weight:
    1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0000
    0's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
17. Code 0000, FFFF relative to midscale (7FFF).
18. Level and Gain DACs both programmed to mid-scale (Code 7FFF).
19. Level and Offset DACs both programmed to mid-scale (Code 7FFF).
20. CPU CK turned off. 256ms delay between measurements. each level tested one at a time.

DC Characteristics - RT-DAC Calibration

All DC tests are performed after the RT-DAC is first calibrated. The upper 5 bits of the RT-DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carries as small as possible.

VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
16510	D15 Step Error	Code 8000 – Code 7FFF – LSB; VR1; Note 21	–5		+5	mV
16520	D14 Step Error	Code 4000 – Code 3FFF – LSB; VR1; Note 22	–5		+5	mV
16530	D13 Step Error	Code 6000 – Code 5FFF –LSB; VR1; Note 23	–5		+5	mV
16540	D12 Step Error	Code 7000 – Code 6FFF – LSB; VR1; Note 24	–5		+5	mV
16550	D11 Step Error	Code 7800 – Code 77FF – LSB ; VR1; Note 25	–5		+5	mV

NOTES:

21. (DAC @ B000 – DAC @ 3000) / (B000 –3000) – DAC LSB; VR1
22. (DAC @ 7000 – DAC @ 3000) / (7000 – 3000) – DAC LSB; VR1
23. (DAC @ 7000 – DAC @ 5000) / (7000 – 5000) – DAC LSB; VR1
24. (DAC @ 7000 – DAC @ 6000) / (7000 – 6000) – DAC LSB; VR1
25. (DAC @ 7800 – DAC @ 7000) / (7800 – 7000) – DAC LSB; VR1

DC Characteristics - RT DAC

There are 3 on-chip internal DACs per channel used for:

1. RT-DAC Level
2. RT-DAC Offset Correction
3. R-DAC Gain Correction

DAC testing is performed post RT-DAC Calibration.

VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V..

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Level DAC Test						
16100	Span	Notes 26, 28	7.6	8.0	8.4	V
16110	Linearity	Notes 26, 29	–5	0	+5	mV
16120	Bit Test	Notes 26, 30	–5	0	+5	mV
16400	RMS DAC Noise Test	FV = 0V; measured at FORCE_A			50	µV
Offset DAC Test						
16200	+Adjustment Range	Notes 26, 31, 32	+5.2	+6.0	+6.6	% of Span
16210	–Adjustment Range	Notes 26, 31, 32	–6.6	–6.0	–5.2	% of Span
16220	Linearity	Notes 26, 29, 32	–5	0	+5	mV
16230	Bit Test	Notes 26, 30, 32	–5	0	+5	mV
Gain DAC Test						
16300	+Adjustment Range	Notes 26, 33	1.07	1.125	1.15	V/V
16310	–Adjustment Range	Notes 26, 33	.850	.875	.922	V/V
16320	Linearity	Notes 26, 31, 33	–2	0	+2	mV/V
16330	Bit Test	Notes 26, 30, 33	–2	0	+2	mV/V
Vmid DAC						
16440	Linearity	Notes 26, 34	–25		+25	mV

NOTES:

26. DAC tests performed using the PMU in FV mode and the MONITOR output VR1.
27. Offset and Gain DACs both programmed to midscale (Code 7FFF).
28. Span = DAC(FFFF) –DAC(0000),
29. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF.
30. Bit Test - Walking 1 and Walking 0 to determine the correct bit weight:
    1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0000
    0's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
31. Code 0000, FFFF relative to midscale (7FFF).
32. Level and Gain DACs both programmed to mid-scale (Code 7FFF).
33. Level and Offset DACs both programmed to mid-scale (Code 7FFF).
34. Linearity Test - 16 codes relative to a straight line determined by 2/16 and 13/16 measurement points: 0000, 0001, 0010, 0011 ... 1100, 1101, 1110, 1111. DAC Code = 7FFF, FV Mode, VR1.

DC Characteristics - Force Voltage

The sequence of events performed for FV testing is:

1. Program FV
2. Force current at FORCE_B
3. Measure the voltage at SENSE.

.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
FV Post Calibration						
14200	Output Force Error	VR0	–5		+5	mV
14201	Output Force Error	VR1	–10		+10	mV
14202	Output Force Error	VR2	–15		+15	mV
14203	Output Force Error	VR3	–25		+25	mV

Range	VR0	VR1	VR2	VR3	VR3
IR0	X	X	X	X	PS_PMIN TP = (16V/0µA) TP = (–3V/0µA) TP = (16V/+512mA) TP = (–3V/–512mA) Cal Pts = 0V, 13V Vmid = 12V
IR1	X	X	X	X	
IR2	X	X	X	X	
IR3	PS_PMIN, No Load TP = –0.5V, 1.5V, 3.5V Cal Pts = 0V, 3V Vmid = 1.5V	PS_PMIN, No Load TP = –1V, 3V, 7V cal Pts = 0V, 5V Vmid = 3V	PS_PMIN, No Load TP = –2V, 6V, 14V Cal Pts = 0V, 10V Vmid = 6V	PS_NMAX TP = (+9V/0µA) TP = (–9V/0µA) TP = (+9V/+512mA) TP = (–9V/–512mA) Cal Pts = .–7V, +7V Vmid = 1V	
IR4	X	X	PS_LOW TP = (7V/0µA) TP = (–6V/0µA) TP = (5V/+128mA) TP = (–6V/–128mA) Cal Pts = –4V, +4V Vmid = 2V	X	X
IR5	X	PS_NMIN, No Load TP = –3.6V to +3.6V in 100mV steps Cal Pts = –2.5V, +2.5V Vmid = 250mV	PS_LOW TP = (7V/0µA) TP = (–6V/0µA) TP = (4V/+512mA) TP = (–5V/–512mA) Cal Pts = –4V, +4V Vmid = 2V	X	X

DC Characteristics - Force Current

The sequence of events performed for FI testing is:

1. Program FI to the desired current
2. Force voltage with external PMU at FORCE_B
3. Measure the current at FORCE_B

FI is calibrated separately for sourcing and sinking current. All FI tests are performed at (VCC_OUT – VEE) / 2.

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V..

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Post Calibration FI Error						
14802	Force Current Error	IR2, Note 35	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
14803	Force Current Error	IR3, Note 35	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
14804	Force Current Error	IR4, Note 36	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
14805	Force Current Error	IR5(a), Note 36	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
14805	Force Current Error	IR5(b), Note 36	–(0.5%FS + 0.5% MV)		+(0.5%FS + 05% MV)	

NOTES:

35. VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V.
36. VCC = +14.75V, VCC_OUT = +7.75, VEE = –7.75V, VDD = +3.25V.

Range	Cal Points	FI Test Points
Sourcing IR2 - IR4 IR5(a) IR5(b)	 0/0.8 • Imax 0/204.8mA 0/204.8mA	 0/+0.5 • Imax/+Imax 0/+128mA/+256mA/+300mA +400mA/+512mA
Sinkng IR2 - IR4 IR5(a)	 0/–0.8 • Imax 0/–204.8mA	 0/–0.5 • Imax/–Imax 0/–128mA/–256mA/–300mA

DC Characteristics - Measure Current

The sequence of events performed for MI testing is:

1. Program FV to the desired voltage
2. Force current with external PMU at FORCE_B
3. Measure the current via the monitor
4. Apply software calibration

MI tested in VR3. MI is calibrated separately for sourcing and sinking current. R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V

Spec #	Parameter	Conditions	Min	Typ	Max	Units
MI (Post Calibration)						
14100	Measure Current Error	IR0, Note 37	–(0.1%FS + 0.1% MV)		+(0.1%FS + 0.1% MV)	
14101	Measure Current Error	IR1, Note 37	–(0.1%FS + 0.1% MV)		+(0.1%FS + 0.1% MV)	
14102	Measure Current Error	IR2, Note 37	–(0.1%FS + 0.1% MV)		+(0.1%FS + 0.1% MV)	
14103	Measure Current Error	IR3, Note 37	–(0.1%FS + 0.1% MV)		+(0.1%FS + 0.1% MV)	
14104	Measure Current Error	IR4, Note 38	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
14105	Measure Current Error	IR5, Note 38	–(0.2%FS + 0.2% MV)		+(0.2%FS + 0.2% MV)	
CMRR						
14140	Maximum CMRR Adj	Notes 37, 39	1.0005			%/V
14141	Minimum CMRR Adj	Notes 37, 40			0.9995	%/V
MI-OS DAC						
14145	MI-OS Resolution	IR0, Note 37	2.2	3.4	5.2	µA/Code
14146	MI-OS Linearity	IR0, Notes 37, 41	–2		+2	µA

NOTES:

37. VCC = +18.75V, VCC_OUT = +18.75, VEE = –4.75V, VDD = +3.25V.
38. VCC = +14.75V, VCC_OUT = +7.75, VEE = –7.75V, VDD = +3.25V.
39. FV Mode, VR3, Iout = 0 - IR5, FORCE = +3V, +11V, Max Code.
40. FV Mode, VR3, Iout = 0 - IR5, FORCE = +3V, +11V, Min Code.
41. 16 equally spaced codes relative to a straight line determined by codes 2 and 13.

Range	Cal Points	FI Test Points
Sourcing		
IR0 - IR4	((VCC_OUT + VEE)/2) @ 0mA /(0.8 • Imax)	((VCC_OUT + VEE)/2)/0mA ((VCC_OUT + VEE)/2)/0.5 • Imax ((VCC_OUT + VEE)/2)/1.0 • Imax
IR5	4V @ 0mA/(0.8 • Imax)	+4V/0mA +4V/+256mA +4V/+512mA
Sourcing		
IR0 - IR4	((VCC_OUT + VEE)/2) @ 0mA/(–0.8 • Imax)	((VCC_OUT + VEE)/2)/0mA ((VCC_OUT + VEE)/2)/–0.5 • Imax ((VCC_OUT + VEE)/2)/–1.0 • Imax
IR5	4V @ 0mA/(–0.8 • Imax)	–4V/0mA –4V/–256mA –4V/–300mA –4V/–400mA

DC Characteristics – Measure Voltage (Monitor)

The sequence of events performed for testing the MONITOR is:

1. Program FV to the desired voltage (in VR3, IR5, Iload = 0)
2. Measure the voltage at SENSE
3. Measure the voltage at MONITOR
4. Apply software calibration to the MONITOR
5. Calculate the difference to determine the error.

R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Central Monitor						
14710	MONITOR HiZ Leakage	Tested at 0V; Notes 42, 43	–15	0	+15	nA
14711	MONITOR HiZ Leakage	Tested at VCC – 2V; ; Notes 42, 43	–25	0	+25	nA
19100	MONITOR Output Impedance	Tested at +5V, Iout = 0µA, 500µA; Note 42		0.5	1.0	KΩ
14720	Voltage Error	MV Test Points; Notes 43, 44	–5		+5	mV
19122	MON_REF Output Impedance	Tested at +5V, Iout = 0µA, 500µA; Note 44		2	3	KΩ
14744	MON_REF HiZ Leakage	Tested at 0V, VDD; Note 42	–100		+100	nA
14741	MON_REF, DUT_GND Error	Notes 44, 45	–15		+15	mV

NOTES:

42. VCC = +19V, VCC-OUT = +19V, VEE = –5V, VDD = +3.3V.
43. VCC = +12V, VCC-OUT = +12V, VEE = –12V, VDD = +3.45V.
44. VCC = +18.75V, VCC-OUT = +18.75V, VEE = –4.75V, VDD = +325V.
45. DUT_GND = ±1V, FV Mode, V-FV = +3V, measured at FORCE relative to GND.

MV Testing	MV Cal Points	MV Test Points
PS_MIN	VEE + 5V, VCC – 5V	–3V, +12V, +16V
MS_NMAX	VEE + 5V, VCC – 5V	–10V, 0V, +9V

DC Characteristics - Voltage Clamp Low

The sequence of events performed for testing the low voltage clamps is:

1. Configure in FI mode, IR5, into no load)
2. Program FI = –1V (–Imax)
3. Program VCL
4. Measure voltage at FORCE_B

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.5V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
14410	Low Voltage Clamp Error	VR1, TPVCL1	–50		+50	mV
14420	Low Voltage Clamp Error	VR2, TPVCL2	–50		+50	mV
14430	Low Voltage Clamp Error	VR3, TPVCL3	–100		+100	mV

Range	Cal Points	Test Points
VR1	0V +5V	–1V +3V +6V
VR2	0V +10V	–2V +6V +12V
VR2	0V +10V	–3V +10V +12V

DC Characteristics - Voltage Clamp High

The sequence of events performed for testing the high voltage clamps is:

1. Configure in FI mode, IR5, into no load)
2. Program FI = .+1V (+Imax)
3. Program VCH
4. Measure voltage at FORCE_B

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.5V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
14460	High Voltage Clamp Error	VR1, TPVCH1	–50		+50	mV
14470	High Voltage Clamp Error	VR2, TPVCH2	–50		+50	mV
14480	High Voltage Clamp Error	VR3, TPVCH3	–100		+100	mV

Range	Cal Points	Test Points
VR0	+1V +5V	+1V +3 +7V
VR1	+1V +10V	+1V +6V +14V
VR2	+1V +15V	+1V +10V +17V

DC Characteristics - Current Clamps

Current clamps are tested in IR5 only. The sequence of events to test the high current clamps is:

1. 10Ω to GND
2. Program FV = +7V
3. Program ICH to the test point
4. Measure the current across the external resistor

The sequence of events to test the low current clamps is:

1. 10Ω to GND
2. Program FV = –7V
3. Program ICL to the test point
4. Measure the current across the external resistor

VCC = +12V, VCC_OUT = +12V, VEE = –12V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0

Spec #	Parameter	Conditions	Min	Typ	Max	Units
14500	High Current Clamp Error	TPICLH	–1.0		+1.0	%FS
13520	Low Current Clamp Error	TPICLL	–1.0		+1.0	%FS

Level	Cal Points	TPVCH
ICH	+200mA +400mA	+100mA +300mA +512mA
ICL	–200mA –400mA	–100mA –300mA –512mA

DC Characteristics - Over-Temperature Alarm

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0 unless otherwise specified.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
16550	Tj-Max Linearity	Notes 46, 47	–10	0	+10	mV
	Temperature Linearity	Note 50	–2	0	+2	°C
	Tj-Max Transfer Function (°C)	Note 50		4		°C/Code
	TJ Output Slope	Note 50		5		mV/°C
	Tj-Max Trip Point	Notes 48, 50		103		°C
16555	TJ HiZ Leakage	Tested at 0V, VDD, Note 49	–100	0	+100	nA

NOTES:
46. All 15 codes tested vs. a straight line determined by codes 2 and 13.
47. Actual vs. theoretical, measured via the monitor.
48. Tj-Max = 0000, die temperature measured through the diagnostic mux.
49. VCC = +19V, VCC_OUT = +19V, VEE = –4.75V, VDD = +3.25V.
50. Limits established by characterization and are not production tested.

DC Characteristics - Kelvin Alarms

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Kelvin Alarm High and Low						
14400	Gain	Note 51	50	150	250	mV/Code
14410	Offset	Note 51	40	150	250	mV
14420	Linearity Error	Note 51	–50		+50	mV
14430	Hysteresis		10	40	100	mV

NOTES:
51. All codes tested vs. a straight line determined by codes 1 and 14.

DC Characteristics - External DAC

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0 unless otherwise specified.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Post Calibration Test						
16510	Overall Accuracy	Notes 52, 53	–400	0	+400	µV
Gain Test						
16390	Maximum Gain	ED-Gain<7:0> = FF Hex; Note 54	1.0001	1.001		V/V
16391	Minimum gain	ED-Gain<7:0> = 7F Hex		0.999	0.9999	V/V
16392	Linearity	Note 55	–300	0	+300	µV/V
16393	Bit Test	Note 56	–300	0	+300	µV/V
16394	Resolution	Note 57	5	6.5	8	(µV/V)/Code
Offset Test						
16290	Maximum Offset	Level<15:0> = FFFF Hex	80	110	150	mV
16291	Minimum Offset	Level<15:0> = 0000 Hex	–150	–110	–80	mV
16292	Linearity	Note 58	–600	0	+600	µV
16294	Span Test	Note 59	200	225	250	mV
16500	External DAC DUT_GND Test	Note 60	–1	0	+1	mV

NOTES:
52. VCC = +11V, VCC_OUT = +11V, VEE = –11V, VDD = +3.25V.
53. 2-point calibration of External DAC function. Measured @ 0V, 1V, 2V, 3V, 4V, 5V and 6V.
54. DAC tests performed in FV mode tested and at FORCE_A.
55. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 7F, 6F, 5F, 4F, 3F, 2F, 1F, 0F, 8F, 9F, AF, BF, CF, DF, EF, FF. Actual measurement vs. straight line determined by the calibration points.
56. Bit Test - Walking 1 and walking 0 to determine the bit weight:
    1's - 40, 20, 10, 08, 04, 02, 01, c0, A0, 90, 88, 84, 82, 81
    0's - 3F, 5F, 6F, 77, 7b, 7D, 7E, BF, DF, EF, F7, FB, FD, FE.
    Actual measurement vs. straight line determined by the calibration points.
57. Gain Span Test: ED-Gain<FF> – ED-Gain<7F>.
58. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF. Actual measurement vs. straight line determined by the calibration points.
59. Offset Span Test - Offset at Level<FFFF> – Level<0000>.
60. DUT_GND = ±200mV, VF = +1.5V. Measured at FORCE_A relative to GND.

DC Characteristics - Resistor Values

VCC = +19V, VCC_OUT = +19V, VEE = –5V, VDD = +3.3V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
On-Chip FET Switches						
	Con-Cint	Note 61		5		KΩ
19108	Con-Cext		3	5	7	KΩ
19109	Tj-OE		300	500	700	Ω
	Con-CapA	Note 61		3		KΩ
	Con-CapB	Note 61		400		Ω
19104	Con-Gang_<0:3>		500	800	1,100	Ω
19102	Con-FA-FB		0.5	1.5	3.0	Ω
19101	Con-EF-FB		1.0	3.0	6.0	Ω
19103	ES-OE		2	3.5	5	KΩ

NOTES:
61. Limits established by characterization and are not production tested.

DC Characteristics - Slew Rate Adjust

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V. 0V to 5V and 5V to 0V swings, measured to 1% of final value. CapA = 820pF, CapB = 390pF, Cext = 3.3nF, Con-Cmin = 1..

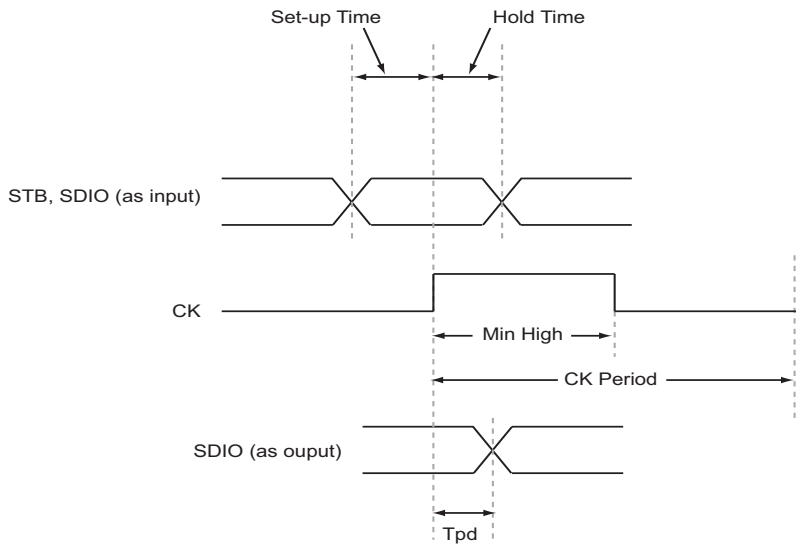
Spec #	Parameter	Conditions	Min	Typ	Max	Units
Settling Times						
26500	**Case 0** Cload = Cmin; Connect CapA, CapB, Cext SR Code = 15; Feedback Point = SENSE		200	400	600	µs
26510	**Case 1 (slowest)** Cload = Cmin; Connect CapA, CapB, Cext SR Code = 0; Feedback Point = FORCE_A		3	6	10	ms
26520	**Case 2** Cload = Cmin; Connect CapA, CapB, Cext SR Code = 15; Feedback Point = FORCE_A		200	400	600	µs
26530	**Case 3 (fastest)** Cload = Cmin; Disconnect CapA, CapB, Cext SR Code = 15; Feedback Point = FORCE_A		5	50	100	µs
26530	**Case 4** Cload = 10µF; Disconnect CapA, CapB; Connect Cext SR Code = 15; Feedback Point = SENSE		200	350	600	µs

AC Characteristics - CPU Port

VCC = +18.75V, VCC_OUT = +18.75V, VEE = –4.75V, VDD = +3.25V, R_EXT = 10KΩ, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Set Up Time						
27100	SDIO to Rising CK		10			ns
27110	STB to Rising CK		10			ns
Hold Time						
27120	SDIO to Rising CK		10			ns
27130	STB to Rising CK		10			ns
Propagation Delay						
27180	Rising CK to SDIO Out	Note 1			10	ns
Pulse Width						
27140	CK Minimum Pulse Width High		22			ns
27150	CK Minimum Pulse Width Low		18			ns
27160	CK Period		50		100	ns
27170	Reset Minimum Pulse Width		100			ns

NOTES:
1. Limits established by characterization and are not production tested.



Chip Overview

Jupiter is a highly integrated system on a chip (SOC) Device Under Test Power Supply (DPS) incorporating all analog and digital functionality required for a single DPS unit for Automatic Test Equipment. The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. One chip constitutes one complete DPS.

CPU Control

All set up, the writing to and reading back of the internal registers and memory is controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating mode of the DPS prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, documents all programmable control signals and their addresses, and shows how to program each internal signal.

High Speed Control

All real time control and observation is accomplished via the real time input and output signals:

- EN (Single Ended Input)
- ALARM* (Single Ended Output)

Analog References

All on-chip analog levels are related to several off-chip precision reference inputs:

- V_REF
- R_EXT

This external reference is used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or part.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

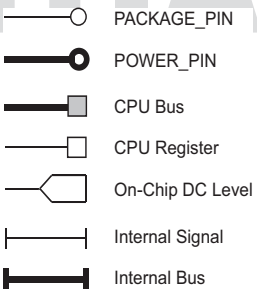
1. All capital letters (i.e. EN, CK, SDIO)
2. Underscores for clarity (i.e. EXT_SENSE, FORCE_A)
3. Shown next to an I/O circle in any schematic.

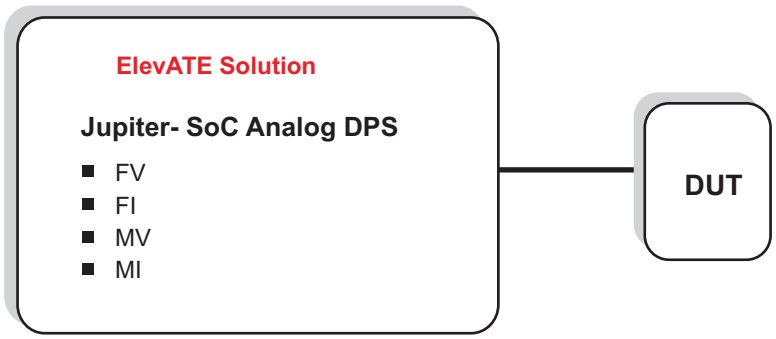
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

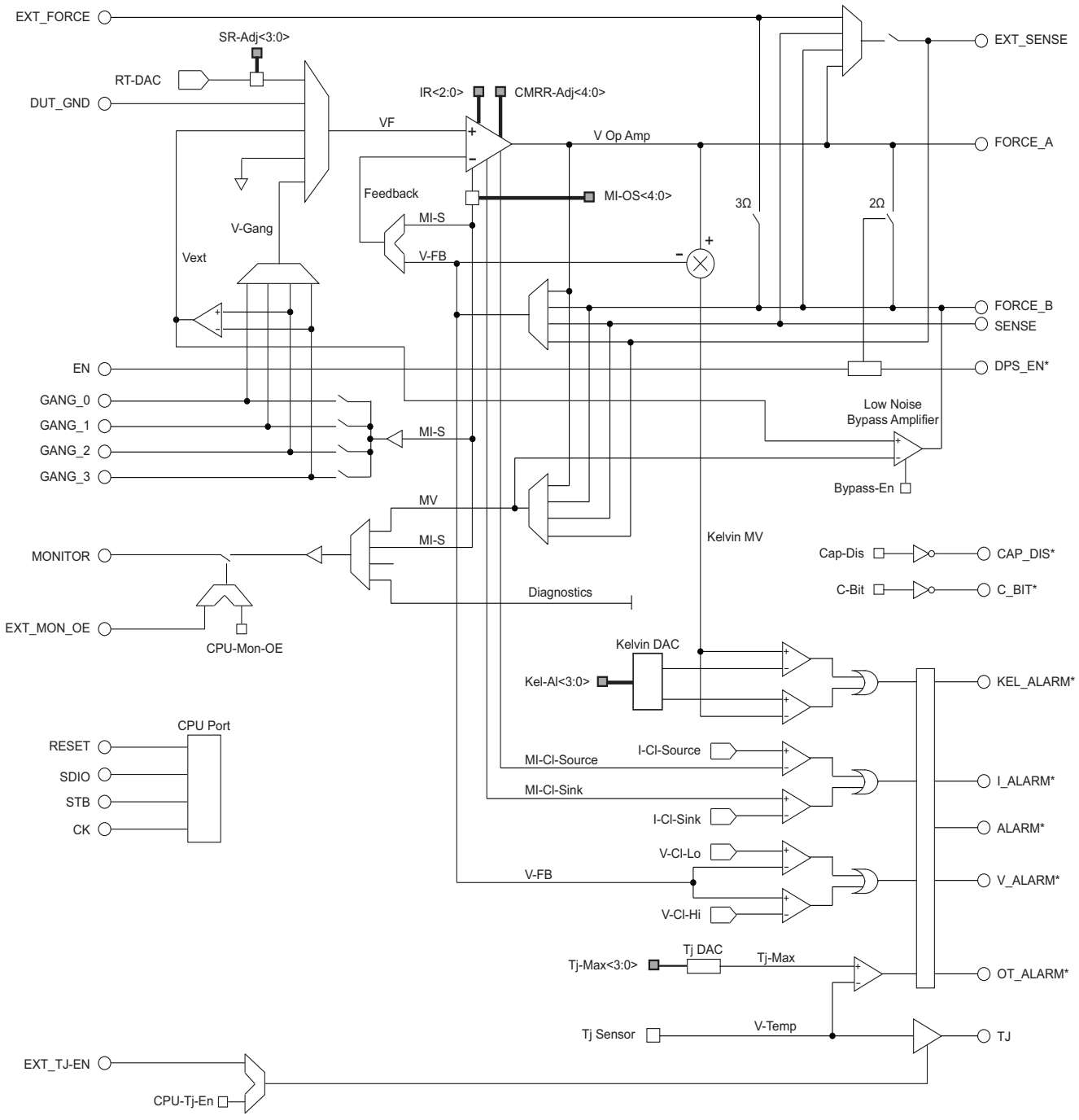
1. The first letter in a word is always a capital letter
2. Subsequent letters within the same word are small
3. Dashes (but never an underscore) for clarity
4. NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.





Detailed Chip Block Diagram

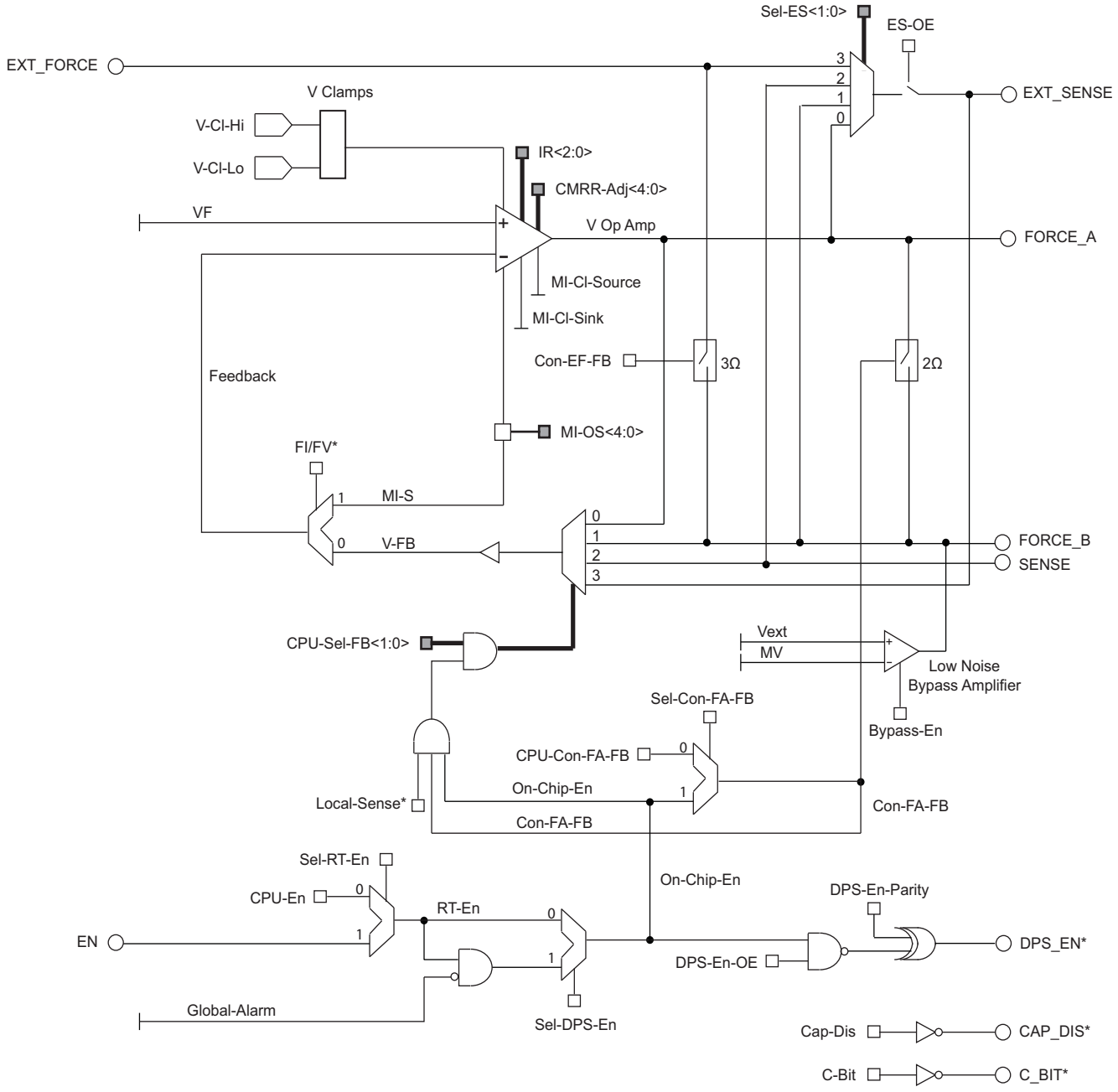


Chip Functionality

Jupiter is a monolithic DUT power supply with the ability to:

- Force Voltage (FV)
- Force Current (FI)
- Measure Voltage (MV
- Measure Current (MI

There are no restrictions between which parameter is being forced and which is being measured.



DPS Configurations

There are two possible DPS configurations:

- Configuration A (No HiZ)
- Configuration B (HiZ)

Configuration A

Configuration A has no on-chip HiZ functionality and FORCE_A is the output. HiZ is performed with an off chip switch (controlled by DPS_EN) or is not performed at all.

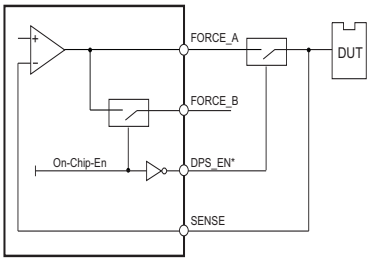


FIGURE 1.

Configuration B

Configuration B supports on-chip HiZ and FORCE_B is the output. HiZ is performed via the on-chip switch controlled by the signal On-Chip-En. Configuration B supports a lower common mode voltage range than does Configuration A, especially in the higher current ranges, due to the voltage drop across the on-chip switch.

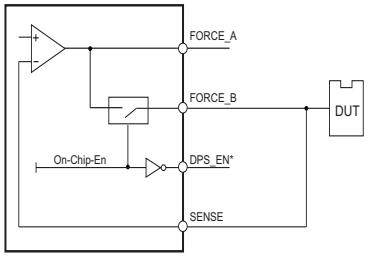


FIGURE 2.

Mode Selection

The CPU port establishes the operating mode of the chip.

TABLE 1.

FI/FV*	Operating Mode
0	FV
1	FI

FV Mode

In FV mode, the DPS wil force a voltage and measure a current at the output pin. There is a 1:1 relationship between the voltage source and the forced voltage at the output.

FV Voltage Source	Voltage at FORCE_A
VF	VF

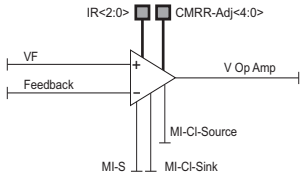


FIGURE 3.

The CPU port selects the current range.

TABLE 2.

IR<2:0>	I Range	MI-S	FV - Imax
000	IR0	±1V	15.625µA
001	IR1	±1V	125µA
010	IR2	±1V	1mA
011	IR3	±1V	8mA
100	IR4	±1V	128mA
101	IR5	±1V	512mA
101	IR5	±2V	1,024mA
110	N/A		N/A
111	N/A		N/A

FI Mode

In FI mode the DPS will force a current and measure a voltage. This mode is particularly useful when testing for continuity on power supply pins when it may be preferable to inject a current to the DUT rather than force a voltage.

TABLE 3.

Level<15:0>	VF	Iout
0000	–1V	–Imax
8000	0	-
FFFF	+1V	+Imax

The CPU selects the current range.

TABLE 4.

IR<2:0>	I Range	MI-S	FV - Imax
000	IR0	±1V	Not Supported
001	IR1	±1V	Not Supported
010	IR2	±1V	±1mA
011	IR3	±1V	±8mA
100	IR4	±1V	±128mA
101	IR5	±1V	±512mA
110	N/A	±1V	N/A
111	N/A	±1V	N/A

MI Mode

When measuring current, MI-S has the following transfer function.

TABLE 5.

MI-S	Iout
–1V	–Imax
0V	0
+1V	+Imax

Over-Current Capability

MI-S is an analog voltage that tracks the current flowing into or out of the part and ±1V corresponds to ± Imax for a selected range. However, MI-S will continue to track the current as the current exceeds Imax until the part can no longer source or sink current or MI-S becomes too close to VCC or VEE and no longer operates properly.

In this manner an Imax of 1.024A may be supported with a MI-S of ±2V.

MI Offset

MI offset adjusts the MI and FI transfer function to be shifted upward or downward by a small amount. This offset correction is useful mainly in the lowest two current ranges (IR0 and IR1) as a means of centering the MI and FI transfer functions at 0V.

MI offset affects the lowest 4 current ranges (IR0 - IR3) only. It has not effect on the highest two current ranges (IR4 - IR5).

TABLE 6.

MI-OS<4>	MI-OS<3:0>	MI Offset
0	1111	–48µA
0	1110	–45µA
•	•	•
0	0001	–3µA
0	0000	0µA
1	0000	0µA
1	0001	+3µA
•	•	•
1	1110	+45µA
1	1111	+48µA

Resolution = 3 µA

CMRR Calibration

The current force (FI) and current measure (MI) transfer functions have a correction register that can be set via the CPU port to adjust the CMRR.

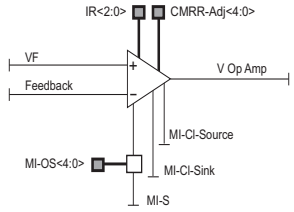


FIGURE 4.

TABLE 7.

CMRR-Adj<4> (Parity)	CMRR-Adj<3:0> (code	CMRR Adjustment
0	1111	1.0015
•	•	•
0	0001	1.0001
0	0000	1.0000
1	0000	1.0000
1	0001	0.9999
•	•	•
1	1111	0.9985

Resolution = 0.1%/V (of Full Scale Current Range)

The default state is 00000, which results in no CMRR adjustment. By setting CMRR-Adj<4:0> correctly, the actual transfer function can more closely track the ideal transfer function.

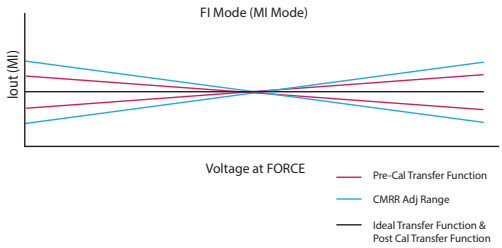


FIGURE 5.

CMRR adjust is performed on MI-S only. MI-CI-Source and MI-CI-Sink may not be calibrated for CMRR.

CMRR-Adj<4:0> should be calibrated independently for each individual current range in order to achieve optimal performance. If IR<2:0> is changed the corresponding CMRR-Adj<4:0> should be set.

FV Feedback Options

In FV mode, the DPS will force a voltage at the selected output node. There are 4 sources of voltages that may be fed back to the forcing op amp. The default condition is the tight loop configuration, which guarantees that the op amp is in a closed loop.

TABLE 8.

Sel-V-FB<1:0>	Feedback	Loop Configuration
00	FORCE_A	Tight Loop/Local Sense
01	FORCE_B	Local Sense B
10	SENSE	Remote Sense
11	EXT-SENSE	Calibration

The CPU can exercise direct control over the feedback selection. However, in cases where the op amp could go open loop the feedback point will automatically go to FORCE_A and local sensing will occur.

TABLE 9.

Local Sense*	On-Chip-En	Con-FA-FB	Local-V-FB<1:0>
0	X	X	00
1	0	X	00
1	1	0	00
1	1	1	CPU-Sel-FB<1:0>

Sel-V-FB<1:0> may be read back by the CPU port.

Configuration Selection

Local Sense* is a CPU register that overrides all other configuration control registers and may be used to guarantee that the forcing op amp does not go open loop. Con-FA-FB and On-Chip-En are both signals that reflect the real time status of the part.

Tight Loop/Local Sense A

The default condition is (upon RESET) the tight closed loop, where the output of the op amp is fed directly back to the inverting input. Tight loop is used to guarantee the op amp will not go open loop.

This configuration is used in applications where there is no remote sense or as a means to keep the op amp in a closed loop when the off chip HiZ switch is opened up.

Local Sense B

This configuration is used in applications where there is no remote sense.

Remote Sense

This configuration is the most common as it creates the most accurate FV situation by sensing the voltage at the DUT.

External Sense

This configuration may be useful during calibration.

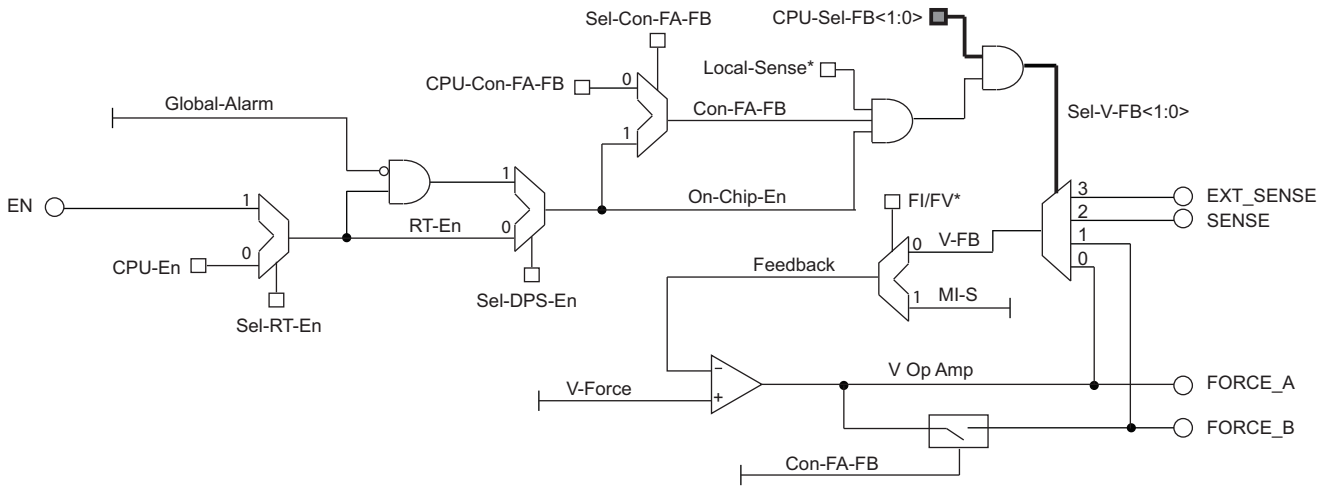


FIGURE 6.

Forcing DAC

Forcing DAC Diagram

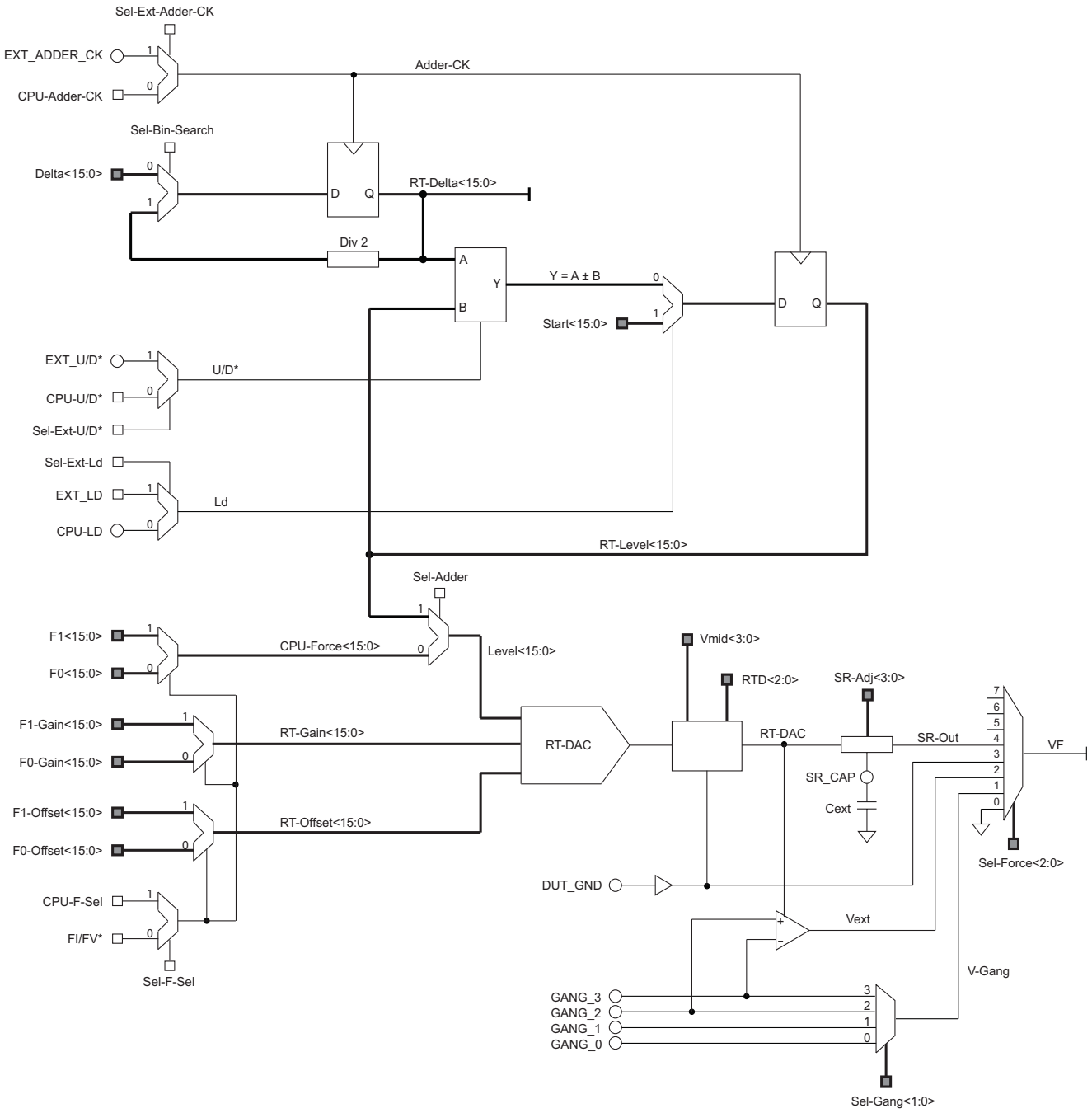


FIGURE 7.

Forcing DAC Voltage Sources

Jupiter supports a wide variety of input voltages that are used to drive the forcing op amp.

On-Chip Resources:

- Real Time DAC
- GND

External Resources:

- GANG_0 - GANG_3
- DUT_GND
- Differential DAC

TABLE 10.

Sel-Force<2:0>	VF
000	Ground
001	V-Gang
010	Buf-DG
011	On-Chip RT-DAC
100	Vext
101 - 111	Not Used

When V-Gang is the selected input, Sel-Gang<1:0> determines which external gang node is used.

TABLE 11.

Sel-Gang<1:0>	V-Gang
#	GANG-#

DUT_GND

DUT_GND is used to correct for any differences between the local chip ground and the ground level at the DUT. All DC levels associated with forcing and measuring voltage at the DUT will be adjusted by the DC value at DUT_GND. DUT_GND has no effect on any DC levels associated with forcing and measuring current.

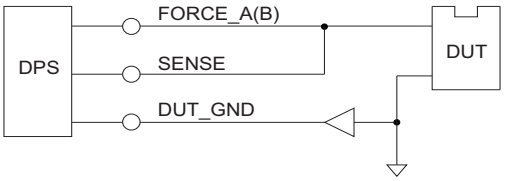


FIGURE 8.

Real Time DAC

There are two sets of on-chip digital codes that may be used as the input to the RT-DAC. The choice between these levels may be controlled directly by the CPU port or by the operating mode of the chip.

TABLE 12.

Sel-F-Sel	F-Sel
0	CPU-F-Sel
1	FI/FV*

Each level has its own independent offset and gain correction, which is useful if F0 is used to force voltage and F1 is used to force current. In such an application FI / FV* can toggle back and forth between modes and both the voltage and the current levels will maintain their calibration values.

TABLE 13.

F-Sel	Selected Forcing Level
0	F0<15:0>
1	F1<15:0>

However, F0 and F1 may also be used to support two distinct voltage levels with the CPU port toggling back and forth between them. In this mode, FI / FV* should not be used as the level select line.

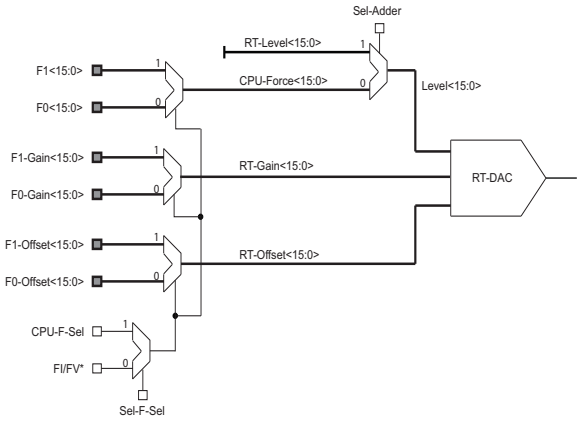


FIGURE 9.

RT-DAC level Generation

In addition to using one of the on-chip RT-DAC forcing levels the RT-DAC level may also be generated algorithmically by an on-chip adder.

TABLE 14.

Sel-Adder	Level<15:0>
0	F0<15:0> or FI<15:0>
1	RT-Level<15:0>

Adder Control

The adder allows the RT-DAC to be stepped up or down by some incremental value. Each positive transition of the adder clock will increase the value of RT-DAC, decrease the value of RT-DAC, or set the value of RT-DAC to the start value.

TABLE 15.

Ld	U/D*	Mode	RT-Level<15:0> (N+1)
0	0	Decrement	RT-Level(N) – RT-Delta<15:0>
0	1	Increment	RT-Level(N) + RT-Delta<15:0>
1	X	Load	Start<15:0>

CPU Read Back

RT-Level<15:0> and RT-Delta<15:0> may be read back through the CPU port.

External Adder Control

The adder is updated on a rising clock edge that may be provided by the CPU port or by an external pin. If CPU control is selected, writing to the CPU-Adder-CK register initiates a one shot pulse going to the adder clock and is a write-only operation.

TABLE 16.

Sel-Ext-Adder-CK	Adder-CK
0	CPU-Adder-CK
1	EXT_ADDER_CK

There is no overflow protection in either the positive or negative direction in that the counter will wrap around if provided enough CK pulses. Therefore, control should be exercised to guarantee that the forced level remains within the desired limits. Adder mode control may be provided by the CPU port or by an external pin.

TABLE 17.

Sel-Ext-U/D*	U/D*
0	CPU-U/D*
1	EXT_U/D*

TABLE 18.

Sel-Ext-Ld	Ld
0	CPU-Ld
1	EXT_LD

Binary Search

The adder supports both a linear and a binary search.

TABLE 19.

Sel-Bin-Search	Adder Mode
0	Linear/Load
1	Binary

In the linear search mode the amount that is added or subtracted from RT-DAC is held constant. In the binary search mode the amount added and subtracted is cut in half after each iteration.

Delta<15:0> is loaded simultaneously with Start<15:0>.

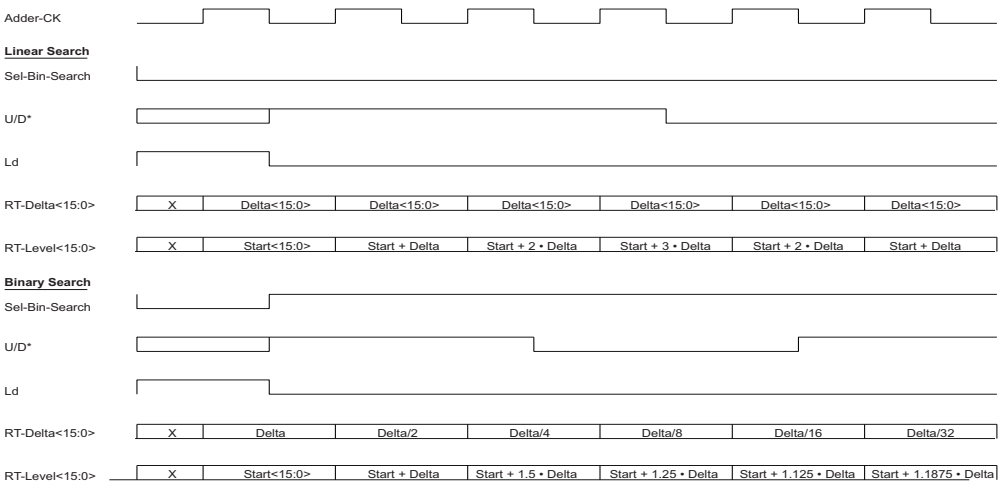


FIGURE 10.

Slew Rate Adjust

The slew rate of the RT-DAC may be adjusted under CPU control. In addition, an internal capacitor and an external capacitor may be connected in order to change the range of slew rate options.

With both switches open the output will have maximum slew rate and minimum slew rate adjust capability. The internal capacitor, external capacitor or both must be connected in order to support adjust slew rate capability.

TABLE 20.

Con-Cint	Con-Cext	Ctotal
0	0	Cnode
1	0	Cnode + Cint
0	1	Cnode + Cext
1	1	Cnode + Cint + Cext

The slew rate is determined by the equation:

dV / dt = Itotal / Ctotal.

Itotal = Imin + Isr-dac

Imin = 1µA

Isr-dac = 10µA • SR-Adj<3:0>

1µA <= Itotal <= 151µA

Nominal capacitance values are:

Cnode = 5pF

Cint = 45pF

Cext = 3,300pF

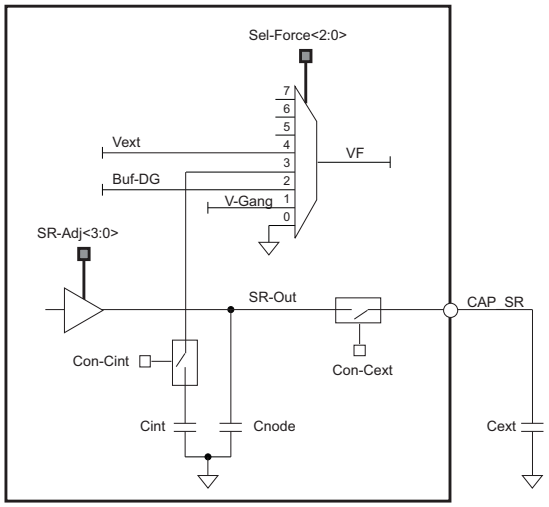


FIGURE 11.

External Forcing DAC

The forcing op amp may be driven by an external differential DAC, typically used in applications where extremely high precision levels are required. The DAC uses gang nodes 2 and 3 as differential inputs, which are then combined into a single ended voltage corrected for DUT_GND.

External DAC Offset Correction

The External DAC can be corrected for offset errors by using the on-chip RT-DAC, scaled down by a factor of 9. RT-DAC must be placed in VIR when used to correct the offset of the External DAC.

TABLE 21.

Level<15:0>	ED-Offset
FFFF (H) FFFE (H) • 8000 (H)	+111mV +110.997mV • 0mV
7FFF (H) • 0001 (H) 0000 (H)	–.0033mV • –111mV –111.003mV

Resolution = 3 µA

External DAC Selection

The CPU port can select the External DAC as the input voltage to the forcing op amp.

TABLE 22.

Sel-Force<2:0>	VF
100	External DAC

Vext = ((GANG_2 – GANG-3) +
(RT-DAC/9)) • ED-Gain<7:0> + DUT_GND

External DAC Gain Correction

The CPU port can correct for any gain errors.

TABLE 23.

ED-Gain<7:0>	Ext-DAC-Gain	Ext-DAC-Gain
01111111 01111110 • 00000001 00000000	–1mV/V –.992mV/V • –7.0µV/V 0	–0.999 0.9990079 • 0.999992 1.0
10000000 10000001 • 11111110 11111111	0 +7.9mV/V • +.992µV/V +1mV/V	1.0 1.0000079 • 1.000992 1.001

Resolution = 7.8 µV/V

Bypass Mode

The main forcing op amp may be bypassed in order to realize the lowest possible noise solution with the following constraints:

1. FV only. No MI capability
2. Iout ≤±10 mA
3. load ≤ 200 pF
4. FORCE_B output used.

In bypass mode, FORCE_A and FORCE_B must be isolated and the bypass op amp must be enabled.

TABLE 24.

Bypass-En	Bypass Op Amp
0	HiZ
1	Active

Bypass Mode Feedback

The bypass op amp uses the MV node as its feedback.

TABLE 25.

Sel-MV<1:0>	MV
00	FORCE_A
01	FORCE_B
10	SENSE
11	EXT_SENSE

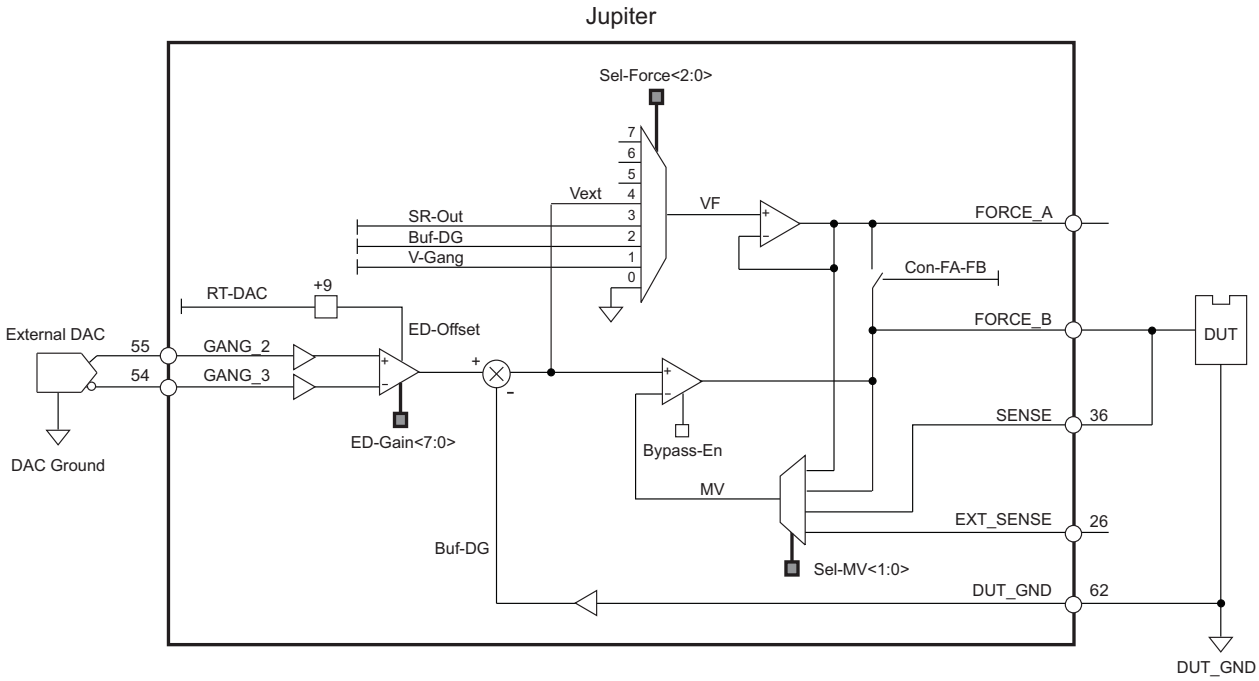


FIGURE 12.

External Force

EXT_FORCE may be connected directly to the FORCE_B pin and indirectly to the FORCE_A pin through the on chip switch between FORCE_A and FORCE_B.

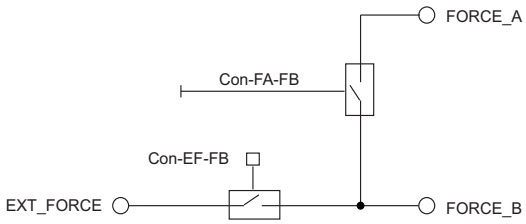


FIGURE 13.

TABLE 26.

Con-EF-FB	Con-FA-FB	EXT_FORCE to FORCE_A	EXT_FORCE to FORCE_B
0	X	Open	Open
1	0	Open	Connectedf
1	1	Connected	Connected

External Sense

EXT_SENSE is a high impedance voltage output pin that provides visibility into several internal nodes.

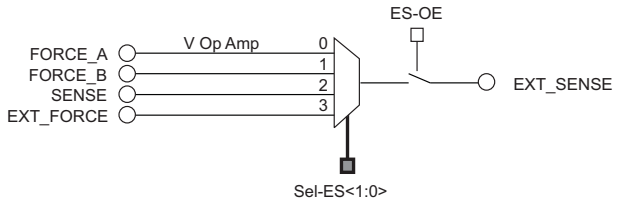


FIGURE 14.

TABLE 27.

Sel-ES<1:0>	EXT_SENSE
00	FORCE_A
01	FORCE_B
10	SENSE
11	EXT_FORCE

EXT_SENSE may be placed into a high impedance state.

TABLE 28.

ES-OE	EXT_SENSE
0	HiZ
1	Active

Monitor

MONITOR / MON_REF are differential analog voltage output pins that provide a real time image of the parameter being measured from the following potential sources:

- MV (measured voltage)
- MI-S (measured current)
- Diagnostics (interior node)

MONITOR and MON_REF are typically connected to an off-chip ADC.

TABLE 29.

Current Measure	MONITOR – MON_REF
+Imax 0 –Imax	+1V 0V –1V
Voltage Measure	
MONITOR – MON_REF = Voltage Measured	

Monitor Reference

MON_REF is the reference signal of MONITOR used as the inverting input to a differential ADC.

TABLE 30.

Sel-Mon-Ref	MON_REF
0 1	Buf-DG Chip Ground

Buf-DG is commonly used when measuring voltages relative to the DUT. Chip Ground is commonly used when measuring currents or voltages local to the chip.

MONITOR Source Selection

The CPU port selects the MONITOR source.

.

TABLE 31.

Sel-Mon<1:0>	MONITOR
00	MV
01	MI-S
10	N/A
11	Diagnostics

If MV is selected, Sel-MV<1:0> controls which node is chosen.

NOTE: MV is also used as the feedback for the low noise external DAC buffer.

TABLE 32.

Sel-MV<1:0>	MV
00	FORCE_A
01	FORCE_B
10	SENSE
11	EXT_SENSE

MONITOR HiZ

MONITOR and MON_REF may be placed into a HiZ state, which is useful when ganging the MONITOR pins from many DPS chips together. Either the CPU port or an external input may be used to control the HiZ state. The external control input allows real time control over MONITOR and MON_REF.

TABLE 33.

Sel-Ext-Mon-OE	CPU-Mon-OE	EXT-MON_OE	Mon-OE	MONITOR MON_REF
0	0	X	0	HiZ
0	1	X	1	Active
1	X	0	0	HiZ
1	X	1	1	Active

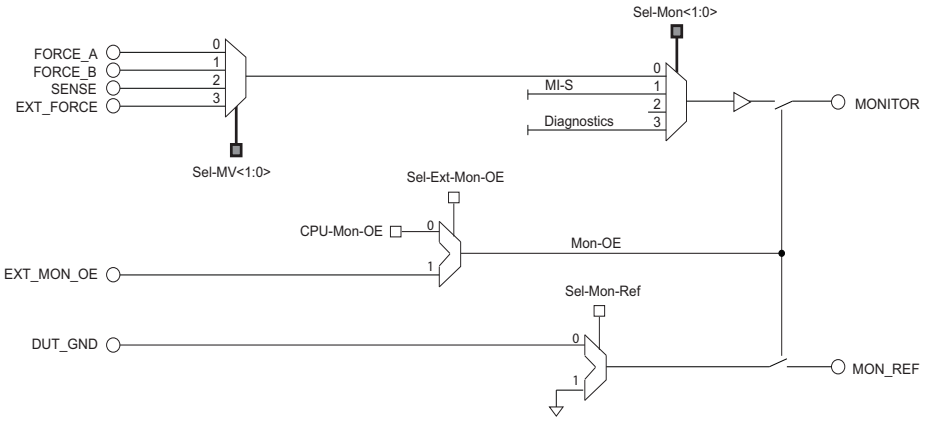


FIGURE 15.

Voltage Clamps

There are programmable voltage clamps that limit the voltage swing at the voltage sense point. These clamps can be used to protect the DUT from an over voltage situation.

The clamps may be turned off by setting V-Cl-En = 0, in which case the clamps will be disabled..

TABLE 34.

V-Cl-En	RT-V-Cl	Voltage Clamps (V-Cl)
0	X	0 (Disabled)
1	0	0 (Disabled)
1	1	1 (Active

When active, the clamps sense the voltage at V-FB. If V-FB is within the limits of the high and low clamps, no action is taken. If V-FB exceeds the high or low voltage clamp the DPS reduces the output current in order for the output voltage to not exceed the clamp. If the voltage at V-FB subsequently drops back to within the clamp levels, the DPS resumes sourcing or sinking its programmed current.

When enabled, the voltage clamps are active in both the FV and FI mode.

CPU Read Back

V-Cl may be read back through the CPU port.

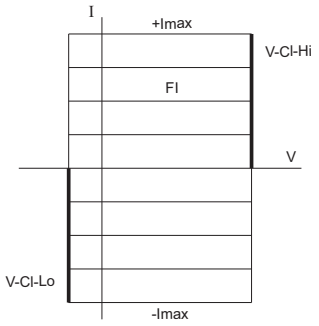


FIGURE 16.

Voltage Alarm

V_ALARM* is an open drain (with a large internal pull up resistor) output that goes low whenever V-Cl is high.

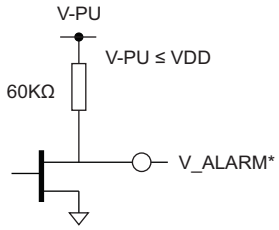


FIGURE 17.

TABLE 35.

V-Cl	V_ALARM*
0	1 (HiZ)
1	0 (Pulling Current)

V_ALARM* may be connected across multiple DPS units to form one voltage alarm signal.

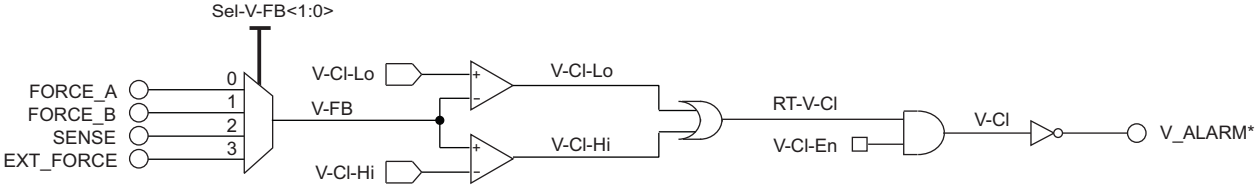


FIGURE 18.

Current Clamps

There are programmable current clamps that limit the current flow. These clamps are useful in protecting the DUT from an over current situation as well as protecting the DPS when the DUT is shorted.

The clamps may be disabled by setting I-Cl-En = 0.

TABLE 36.

I-Cl-En	RT-I-Cl	Current Clamps (I-Cl)
0	X	0 (Disabled)
1	0	0 (Disabled)
1	1	1 (Active

When Active, the I-Clamps sense the current at the output. If the current is within the boundaries set by I-Cl-Hi and I-Cl-Lo, no action is taken. If the measured current exceeds the upper or lower current clamp the DPS reduces the output voltage in order for the output current to not exceed the clamp. If the current drops back to within the clamp levels the DPS resumes forcing its programmed voltage.

When active, the current clamps function in both the FI and FV mode.

Short Circuit Limit

In FV mode, there is a hard output current limit of ~1.2A that is not programmable and may not be disabled.

CPU Read Back

I-Cl may be read back through the CPU port.

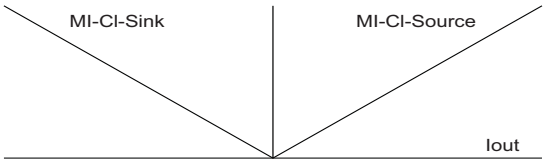


FIGURE 19.

MI-Cl-Source and MI-Cl-Sink track the current flow, are always in the high current range and are independent of the MI-S signal. The current clamps are scaled to cover 2X the high current range.

The high and low current clamps detect current flow in one direction each

.

TABLE 37.

I-Cl-Source<15:0>	I Clamp Level	MI-Cl Source
0000H FFFFH	0mA +1.2A (sourcing)	0V +2V

I-Cl-Sink<15:0>	I Clamp Level	MI-Cl Sini
0000H FFFFH	0mA –1.2A (sourcing)	0V +2V

Current Alarm

I_ALARM* can be a real time signal that comes and goes as the part hits the clamp limit or instead it can be a latched signal that records whether any current limit violation has occurred. The latched bit remains high until cleared by the CPU port.

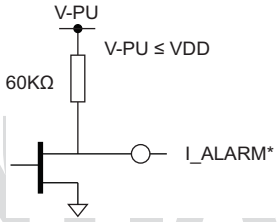


FIGURE 20.

TABLE 38.

Sel-L-I-Cl	I-Cl
0	En-I-Cl
1	L-I-Cl

I_ALARM* is an open drain output (with a large internal pull up resistor) that pulls current when low and goes into a high impedance state when high. I_ALARM* may be connected across multiple DPS units to form one current alarm signal.

TABLE 39.

I-Cl	I_ALARM*
0	HiZ
1	Pulling Current

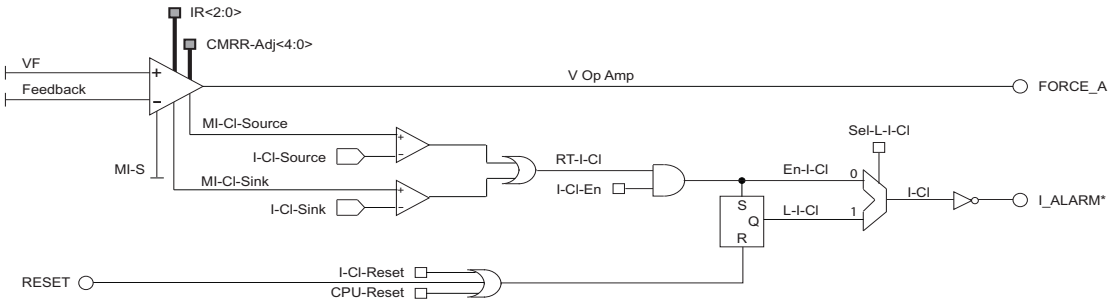


FIGURE 21.

Thermal Alarm

An on-chip thermal monitor allows the chip to detect an over temperature situation and react to that condition. The over temperature flag can be disabled by the CPU port. If enabled, OT reflects the status of the die temperature. Global-OT records if any real time over-temperature failures have occurred. OT-Flag can be used to control the HiZ function in real time.

TABLE 40.

Input Condition	Output Condition
V-Temp < Tj-Max	OK
V-Temp > Tj-Max	OT Fault

Tj-Max<3:0>	Tj-Max
0000	100°C
0001	104°C
0010	108°C
0011	112°C
0100	116°C
0101	120°C
0110	124°C
0111	128°C
1000	132°C
1001	136°C
1010	140°C
1011	144°C
1100	148°C
1101	152°C
1110	156°C
1111	Force Fault

CPU Control

The CPU port can force an over temperature state by programming Tj-Max to its maximum value.

TABLE 41.

CPU-OT-Flag-Dis	CPU-OT	OT	En-OT
1	X	X	0
0	0	0	0
0	1	X	1
0	X	1	1

OT_ALARM* is an open drain output (with a large internal pull up resistor) that pulls current when low and goes into a high impedance state when high.

TABLE 42.

OT-Flag	OT_ALARM*
0	1 (HiZ)
1	0 (Pulling Current)

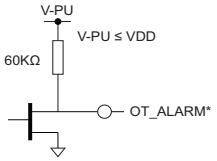


FIGURE 22.

CPU Read Back

OT-Flag may be read back through the CPU port.

Thermal Alarm Reset

Once Global-OT is set it will remain set until cleared by an external hardware RESET, a CPU hardware reset or by the CPU port executing an OT-Flag-Reset. OT-Flag-Reset is a write only transaction and may not be read back by the CPU port.

Temperature Monitor

TJ is a low voltage analog voltage output that tracks the junction temperature. TJ may be placed in a high impedance state by either an external pin or by the CPU port.

TABLE 43.

TJ-OE	TJ
0	HiZ
1	V-Temp

Sel-TJ-En	TJ-OE
0	CPU-Tj-En
1	EXT_TJ_OE

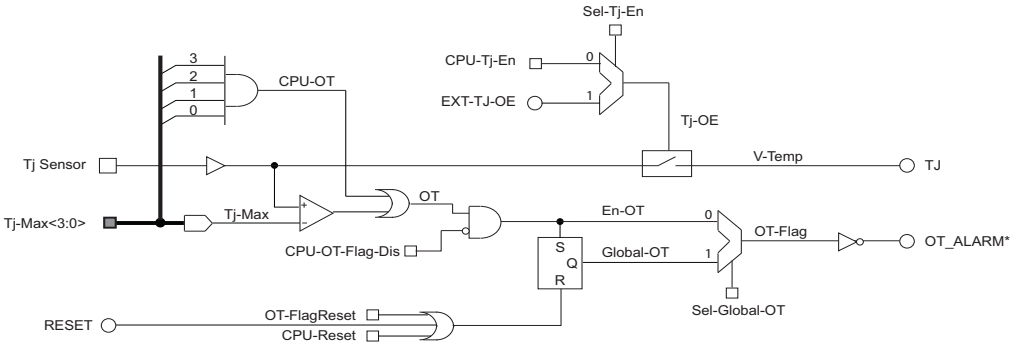


FIGURE 23.

Junction Temperature Monitor

TJ is an analog voltage output that tracks the on-chip junction temperature of the die.

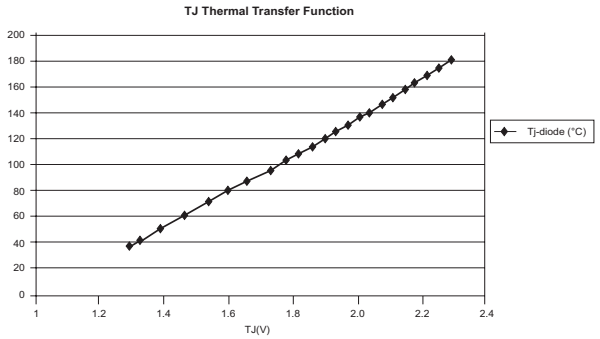


FIGURE 24.

Kelvin Alarm

The Kelvin alarm is set up to detect a discontinuity between the FORCE_A and voltage feedback nodes when in the FV mode. The alarm is set whenever the voltage being forced moves too far away from the voltage being sensed.

TABLE 44.

Kel-Al<3:0>	Kel-Al-Lo	Kel-Al-Hi
0000	-150mV	+150mV
0001	-300mV	+300mV
0010	-450mV	+450mV
0011	-600mV	+600mV
0100	-750mV	+750mV
0101	-900mV	+900mV
0110	-1.05V	+1.05V
0111	-1.2V	+1.2V
1000	-1.35V	+1.35V
1001	-1.5V	+1.5V
1010	-1.65V	+1.65V
1011	-1.8V	+1.8V
1100	-1.95V	+1.95V
1101	-2.1V	+2.1V
1110	-2.25V	+2.25V
1111	-2.4V	+2.4V

TABLE 45.

Input Condition	Kel-Lo	Condition
FORCE_A – V-FB > Kel-Al-Lo	0	OK
FORCE_A – V-FB < Kel-Al-Lo	1	Kelvin Alarm

Input Condition	Kel-Hi	Condition
FORCE_A – V-FB < Kel-Al-Hi	0	OK
FORCE_A – V-FB > Kel-AlHi	1	Kelvin Alarm

KEL_ALARM* is an open drain output (with a large internal pull up resistor) that pulls current when low and goes into a high impedance state when high. KEL_ALARM* may be connected across multiple DPS units to form one Kelvin alarm signal.

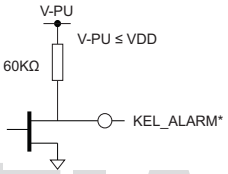


FIGURE 25.

TABLE 46.

Kel-Al	KEL_ALARM*
0	1 (HiZ)
1	0 (Pulling Current)

CPU Read Back

Kel-Al may be read back through the CPU port.

Kelvin Alarm Enable

The CPU port enables both the real time Kelvin flag and the global Kelvin alarm. RT-Kel-Al indicates the real time status of the Kelvin alarm and Global-Kel-Al records whether any real time alarms have occurred.

TABLE 47.

Sel-Global-Kel	Kel-Al
0	RT-Kel-Al
1	Global-Kel-Al

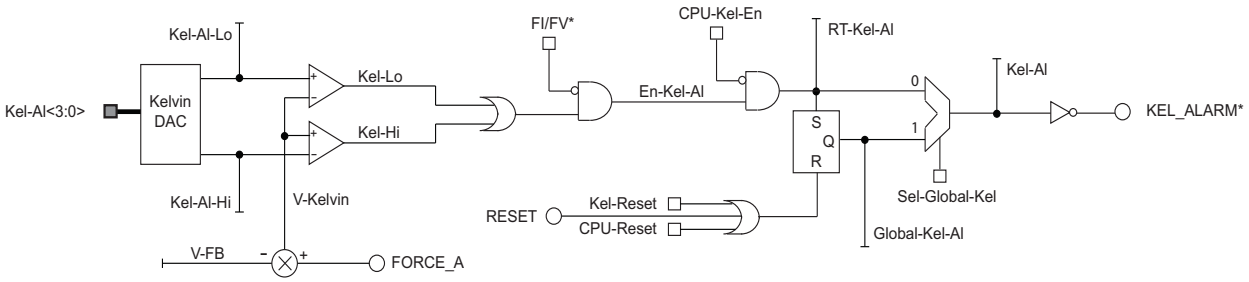


FIGURE 26.

Kelvin Alarm Reset

Once Global-Kel-Al is set it will remain set until cleared by an external hardware RESET, a CPU hardware reset, or by the CPU port executing a Kel-Reset, which activates a one shot to clear the register.

Kel-Reset is a write only transaction and may not be read back by the CPU port.

Protective Shut Down Options

The device can be configured to shut down automatically in case of an:

- over-current situation
- over-temperature situation
- over-Kelvin situation

The CPU can configure any or all of these flags to immediately place the DPS into a HiZ state.

DPS Enable

The on-chip DPS enable may be selected from 3 different sources.

TABLE 48.

I-Cl • CPU-OI-En	OT-Flag * CPU-OT-Dis*	Kel-Al • CPU-OK-En	Global-Alarm	ALARM*
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
0	0	0	0	1

ALARM* is an open drain output (with a large internal pull up resistor) that indicates any type of alarm h has occurred.

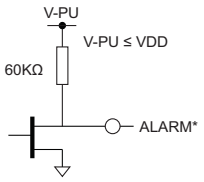


FIGURE 27.

CPU Read Back

Global-Alarm may be read back through the CPU port.

TABLE 49.

Sel-DPS-En	Sel-RT-En	On-Chip-En
1	X	RT-En • Global-Alarm*
0	0	CPU-En
0	1	EN

On-Chip HiZ

DPS configuration B supports on-chip HiZ by opening a switch between the forcing op amp (which drives FORCE_A) and FORCE_B.

TABLE 50.

Sel-Con-FA-FB	CPU-Con-FA-FB	On-Chip-En	Con-FA-FB	DPS Status
0	0	X	0	HiZ
0	1	X	1	Active
1	X	0	0	HiZ
1	X	1	1	Active

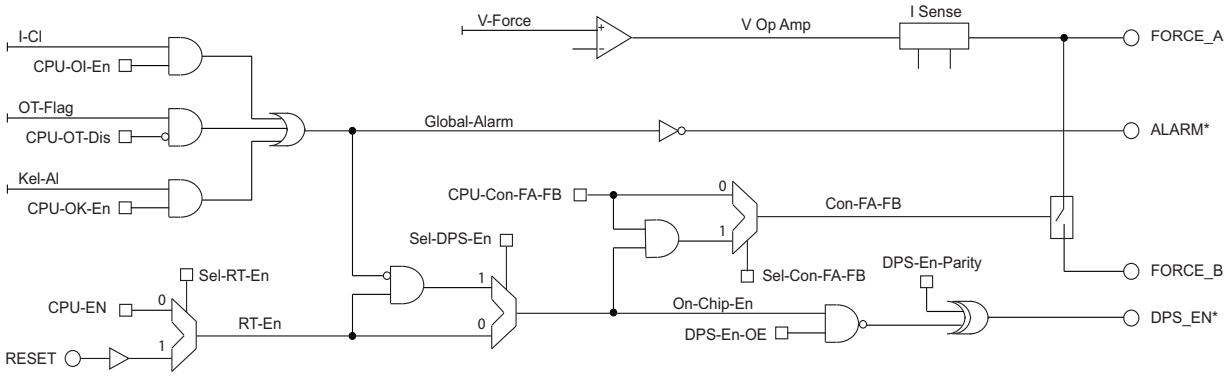


FIGURE 28.

External DPS Enable

In DPS configuration A, where HiZ is implemented off chip, DPS_EN* is an open drain digital output that controls the external switch. A series XOR gate supports either polarity at the signal. The CPU port can gate DPS_EN* signal via DPS-En-OE.

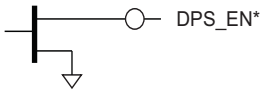


FIGURE 29.

TABLE 51.

DPS-En-OE	On-Chip-En	DPS-En-Parity	DPS_EN*
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Low Current Applications

In order to quickly take low current measurements, the off chip capacitor located at the DUT may be disconnected via the control bit output signal CAP_DIS*.

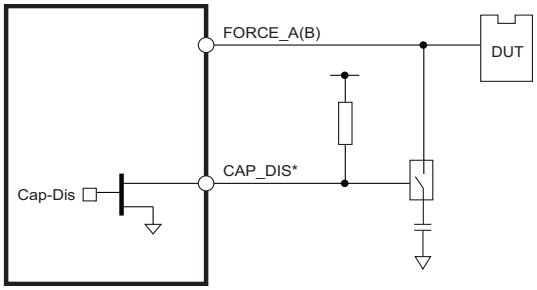


FIGURE 30.

TABLE 52.

Cap-Dis	CAP_DIS*
0	1 (HiZ)
1	0 (Pulling Current)

CAP_DIS* is an open drain output up that requires an external pull up resistor to realize a high state.

DUT Capacitive Loads

The part is designed to be stable over an extremely wide range of load conditions. There are different values of compensation that can be switched in to match up better with different values of loads.

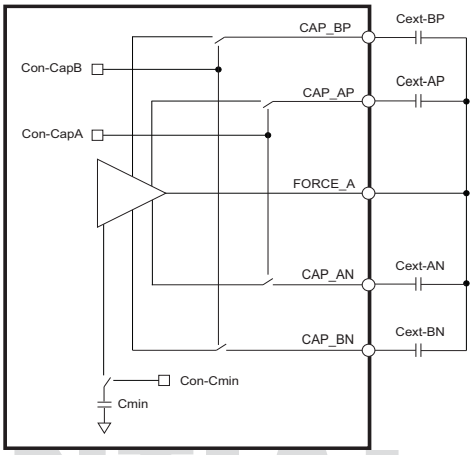


FIGURE 31.

TABLE 53.

Con-CapA, Con-CapB	Cload Maximum
00	1µF
11	50µF

Con-CapA and Con-CapB must be programmed to equal values in that only both or neither can be connected. The relationship between the capacitor values is:

Cext-BP, Cext-BN = 0.5 • (Cext-AP, Cext-AN).

Typical external cap values are:

Cext-AP, Cext-AN = 820 pF

Cext-BP, Cext-BN = 390 pF.

However, different capacitor values can be used to trade off stability under a capacitive load vs. settling time.

Low Capacitive Load Compensation

A minimum amount of compensation capacitance may be added in applications where Cload < 20 nF in order to guarantee stability.

TABLE 54.

Cload	Con-Cmin
<20nF	1
>20nF	0

For applications with larger capacitive loads, Cmin should NOT be connected as it needlessly adds phase shift.

High Current Applications

Each individual DPS supports a maximum current up to 1A. However, multiple DPS units may be ganged together in FV mode in order to create one DPS unit but with higher maximum current.

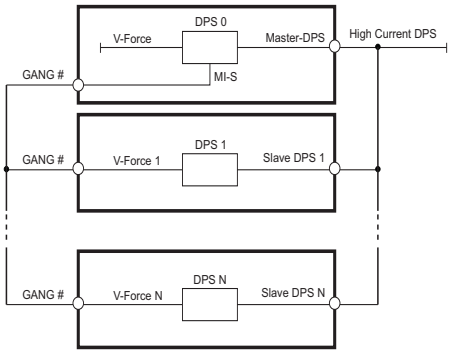


FIGURE 32.

High Current FV / MI

To create a high current FV / MI source, the following steps are taken:

- Select a master DPS and place it in FV mode.
- Connect the master MI-S signal to one of the GANG_# (GANG_0 - GANG_3) nodes.
- Select all slave DPS units and place them in FI mode.
- Select GANG_# as the forcing voltage for all slave units.

The maximum output current is the sum of the individual output currents of the master and all slave DPS units. To achieve this high current rating, the FORCE_A or FORCE_B pins must be connected off chip.

Ganging Options

There is no restriction on how many independent DPS units may be ganged together and it is therefore possible to implement very high current DPS supplies.

There are a total of 4 independent ganging nodes supported per chip. If more than 4 ganged supplies need to be provided for within a tester, and additional off chip ganging matrix must be constructed to allow for greater ganging node routing flexibility.

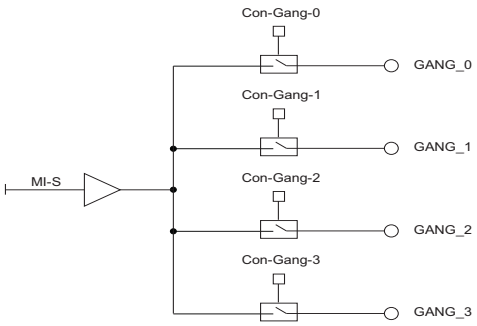


FIGURE 33.

Gang nodes may be connected directly together across multiple DPS units without the need for additional off-chip circuitry. Default condition for the ganging control bits (upon power up and reset) is a logical 0 and places the ganging nodes in a high impedance state.

TABLE 55.

Con-Gang-#	GANG_#
0	HiZ
1	MI-S

MI-S may be routed independently to any of the ganging nodes GANG_0 - GANG_3. The CPU port controls the ganging selection.

Diagnostic Options

The measurement unit has access to many key internal nodes, which may be brought out via the MONITOR through the Diagnostic node under CPU port control.

This visibility is used typically during test, characterization and calibration.

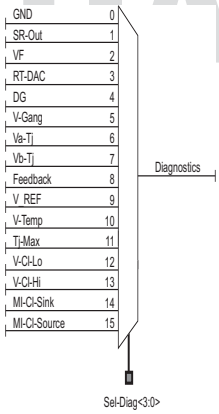


FIGURE 34.

Spare Control Bit

C_BIT* is an output pin that provides an extra control bit, under CPU port control, for external circuit. C_BIT* is a generic bit in that is can be used for any external function.

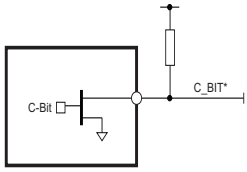


FIGURE 35.

TABLE 56.

C-Bit	C_BIT*
0	1 (HiZ)
1	0 (Pulling Current)

C_BIT* is an open drain output that requires an external pull up to realize a high state.

DC Levels

Different functional blocks require DC voltage levels in order to function properly. These levels are all generated on chip with a 16 bit DAC that is programmed through the CPU port.

There are 5 voltage range options. Various DC levels are grouped together and the selected voltage range is common for all levels within each group. (See table below)

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2 and VR3. If a level is programmed beyond what the power supply levels support saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options vs. Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

TABLE 57.

Range Select<2:0>	Voltage Range	Resolution (LSB)	Full Scale (FS)
0	VR0	61µV	4
1	VR1	122µV	8
2	VR2	244µV	16
3	VR3	488µV	32
4	VIR	30.5µV	2
5-7	N/A	-	-

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a % of the full scale voltage range of each particular voltage group.

TABLE 58.

Offset Code	Offset Value	Gain Code	Gain Value
0000H	–5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. DUT_GND is common for all channels within a package and is super imposed upon all voltage levels generated on the chip.

The input at DUT_GND should be:

1. filtered for noise
2. stable
3. reflect the actual ground level at the DUT

V_REF

V_REF is an analog input voltage that is used to program the on chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels on the same chip.

V_REF Sensitivity

The above equations that predict the DAC output assume that V_REF = 3.000V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio.

Offset adjust has ample range to correct for deviations in V_REF, in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from 3.0V will not affect DC accuracy.

Adjustable Vmid

To support applications that require a wide variety of voltage range options, the value for Vmid in the output level calculation is programmable. This adjustment allows the same total voltage swing in each of the different voltage ranges, only now that voltage span may be adjusted more positive or more negative.

The setting of the Vmid register has no effect on FI mode or on the I Clamps.

TABLE 59.

Voltage Range	Vmid LSB	Vmid<3:0>	Vmid
VR0	125mV	0000 1111	+125mV +2.0V
VR1	250mV	0000 1111	+250mV +4.0V
VR2	500mV	0000 1111	+500mV +8.0V
VR3	1V	0000 1111	+1V +16V

Voltage Range Table

Several examples of different voltage ranges are shown Table 60 below. For simplicity in each example:

- Gain Correction = 1.0
- Offset Correction = 0.0V
- DUT_GND = 0.0V.

Level Programming

Voltage ranges VR0, VR1, VR2 and VR3 use the equation:

Vout = (Value - Vmid) • Gain + Offset + Vmid + DUT_GND

Current force mode (VIR) uses the equation:

Vout = (Value - Vmid) • Gain + Offset + Vmid

Value is described by the equation:

Value = {(DAC Code) / (2**N - 1)} • FS + Vmid – (FS / 2)
N = 16; 2**N - 1 = 65,535

The voltage range lower and upper limits are:

Vmin = Vmid - (FS / 2)
Vmax = Vmin + FS

For FI mode:

FS = 2V
Vmin = –1V
Vmid = 0V
Vmax = +1V

For I Clamps:

FS = 2V
Vmin = 0V
Vmid = 1V
Vmax = 2V

TABLE 60.

Range	FS	Vmid<3:0>	Vmid Value	DAC Code	Output Voltage
VR0	4	0000	+0.125V	0000 Hex FFFF Hex	–1.875V +2.215V
VR0	4	1011	+1.5V	0000 Hex FFFF Hex	–0.5V +3.5V
VR0	4	1111	+2V	0000 Hex FFFF Hex	0V +4V
VR1	8	0000	+0.25V	0000 Hex FFFF Hex	–3.75V +4.25V
VR1	8	1111	+4V	0000 Hex FFFF Hex	0V +8V
VR2	16	0000	+0.5V	0000 Hex FFFF Hex	–7.5V +8.5V
VR2	16	1111	+8V	0000 Hex FFFF Hex	0V +16V
VR3	32	0000	+1V	0000 Hex FFFF Hex	–15V +17V
VR3	32	1111	+16V	0000 Hex FFFF Hex	0v +32V

DC Level Range Options

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in the table below.

TABLE 61.

Range Decode						
Internal DC Levels	**VR0**	**VR1**	**VR2**	**VR3**	**VIR**	**Range Select Bits <1:0>**
Real Time DAC **RT-DAC**	√	√	√		√	RTD<2:0>
Voltage Clamps **V-Cl-HI, V-Cl-Lo**		√	√	√		VCI<2:0>
Current Clamps **I-Cl-HI, I-cl-Lo**					√	N/A
Tracks DUT_GND (FV, MV)						
Does NOT Track DUT_GND (FI, MI)						

DC Level Test Procedure

The part is designed and tested to meet its DC accuracy specifications after a two point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. However, most calibration points will be at 20% and 80% of the full scale value for that range.

The test points are broken into two categories:

1. inner test
2. outer test

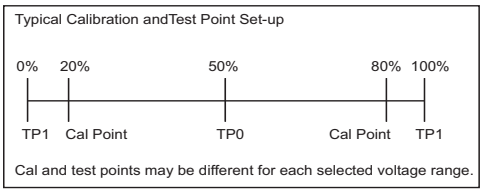


FIGURE 36.

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

.

SYSTEM LEVEL DC ACCURACY LIMITS

Other calibration schemes and techniques, using different, more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the Offset DAC
4. Calibrate the Gain DAC
5. Calibrate the DC Level

LEVEL CALIBRATION

Initialize

- Select desired voltage range (VR0, VR1, VR2, VR3, VIR)
- Set Gain = 1.0; Offset = 0.0V

Measure

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

Calculate

- Gain' = (Output2'– Output1') / (Level 2 – Level1)
- Offset' = (Output2' - Vmid) - Gain' o (Level2 – Vmid)

Finish

- Set Offset = –Offset' / Gain'
- Set Gain = 1.0 / Gain'

Real Time DAC Calibration

To facilitate superior DC accuracy, the RT DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction..

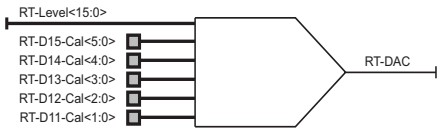


FIGURE 37.

TABLE 62. D15 Calibration

RT-D15-Cal5	RT-D15-Cal4	RT-D15-Cal3	RT-D15-Cal2	RT-D15-Cal1	RT-D15-Cal0	D15 Adjustment
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 63. D14 Calibration

RT-D14-Cal4	RT-D14-Cal3	RT-D14-Cal2	RT-D14-Cal1	RT-D14-Cal0	D14 Adjustment
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	– 3LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 64. D13 Calibration

RT-D13-Cal3	RT-D13-Cal2	RT-D13-Cal1	RT-D13-Cal0	D13 Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 65. D12 Calibration

RT-D12-Cal2	RT-D12-Cal1	RT-D12-Cal0	D12 Adjustment
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 66. D11 Calibration

RT-D11-Cal1	RT-D11-Cal0	D11 Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3LSB

Static DC Level Calibration

There is a 16 bit DAC used to generate the required DC support levels. To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

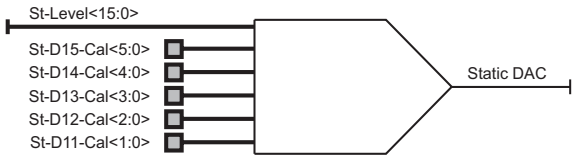


FIGURE 38.

TABLE 67. D15 Calibration

St-D15-Cal5	St-C15-Cal4	St-D15-Cal3	St-D15-Cal2	St-D15-Cal1	St-D15-Cal0	D15 Adjustment
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 68. D14 Calibration

St-D14-Cal4	St-D14-Cal3	St-D14-Cal2	St-D14-Cal1	St-D14-Cal0	D14 Adjustment
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	– 3LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 69. D13 Calibration

St-D13-Cal3	St-D13-Cal2	St-D13-Cal1	St-D13-Cal0	D13 Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 70. D12 Calibration

St-D12-Cal2	St-D12-Cal1	St-D12-Cal0	D12 Adjustment
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 71. D11 Calibration

St-D11-Cal1	St-D11-Cal0	D11 Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3LSB

Required External Support

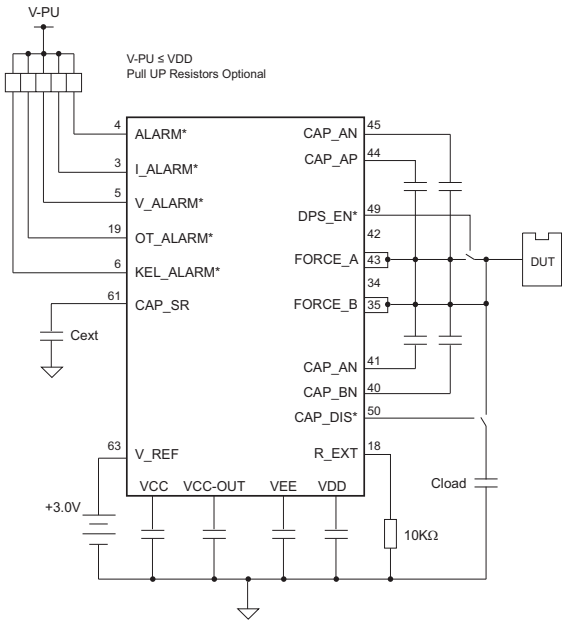


FIGURE 39.

V_REF

V_REF is an analog input voltage that is used to program the on chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

R_EXT

R_EXT is a stable precision external resistor with a low temperature coefficient.

External Pull Up Resistors

Outputs V_ALARM*, I_ALARM*, KEL_ALARM*, OT_ALARM* and ALARM* are all open drain output pins with an internal pull up resistor and therefore may, or may not, require an external pull up resistor to some positive voltage (<= VDD) to function properly.

C_BIT*, CAP_DIS* and DPS_EN* are open drain outputs and therefore requires an external pull up resistor to some positive voltage to function properly.

Power Supply Restrictions

The following guidelines must be met to ensure proper operation:

1. VCC ≥ GND
2. VEE ≤ GND
3. VDD ≥ GND
4. VDD ≥ VREF
5. VCC ≥ VDD
6. VCC ≥ VCC_OUT

Schottky diodes on a once per board basis are recommended to protect against a power supply restriction violation.

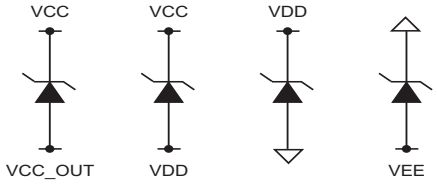


FIGURE 40.

Power Supply and Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while meeting the power supply restrictions. However, since achieving that power up condition may be difficult, the following sequence is recommended:

1. VEE
2. VCC
3. VCC_OUT
4. VDD
5. V_REF

CPU - Overview

All on chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low before another transaction may begin.

Clock Requirements

Even if no CPU transactions are occurring, CK is used on chip for other functions and therefore should toggle continuously for correct chip operation. If the clock is turned off, the voltage and current clamp levels will not be refreshed and may not hold DC accuracy.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached. Each group of registers with a common WE is shown in the memory map tables with a common background color.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don't care (X) value.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 72.

1st SDIO Bit	CPU Transaction Type
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Unused data bits are read back as a don't care (X) state.

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs. Since there is only 1 channel per IC the parallel bit should always be programmed to 0.

Reset

RESET is an external hardware reset signal that places all internal registers into a low state. Reset must be executed after a power up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.**

RESET is active high.

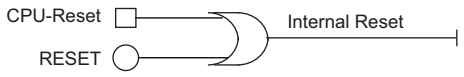


FIGURE 41.

In addition, the CPU port can execute a reset (as a write only transaction.) If the Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Chip ID

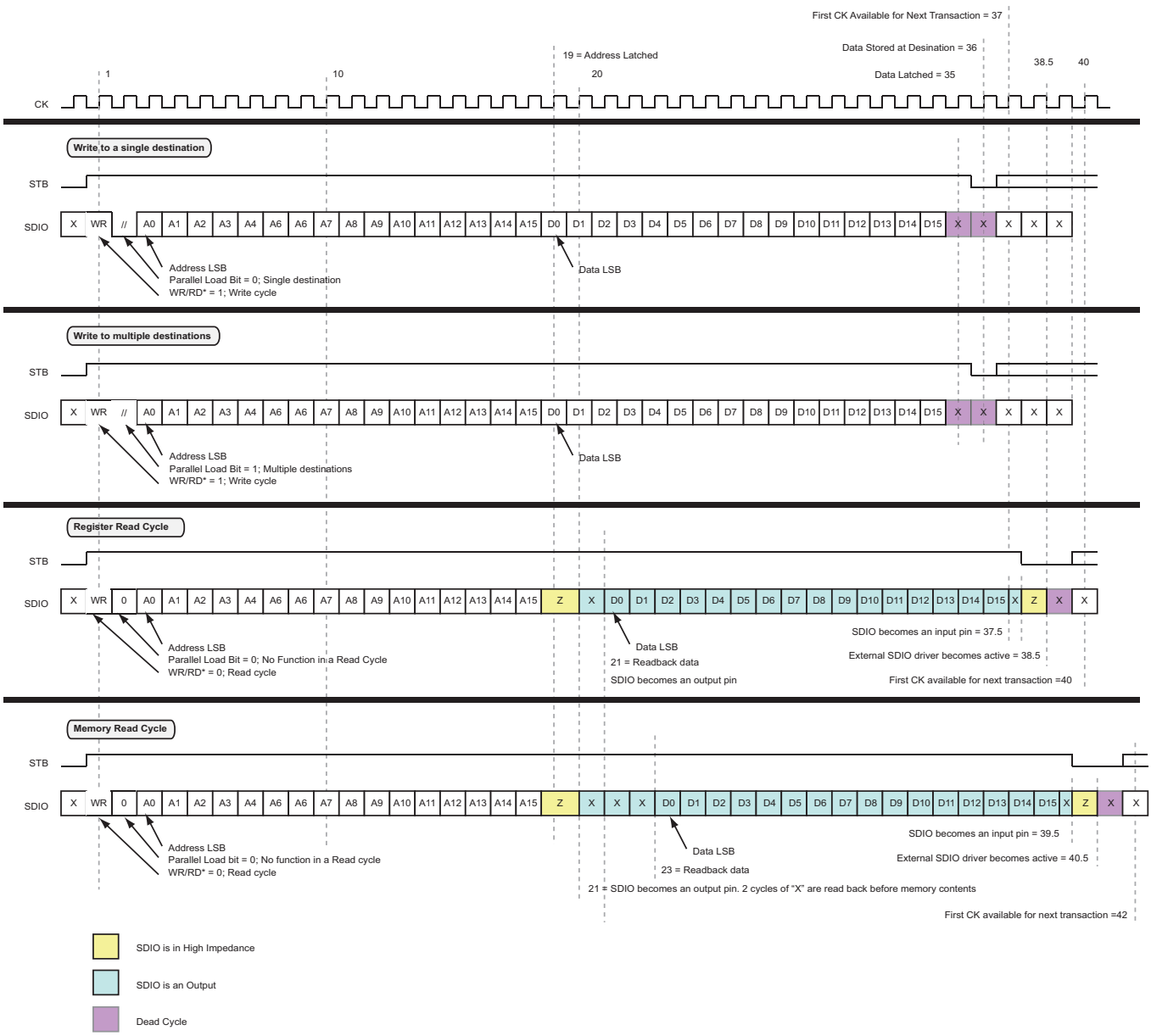
Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 73.

SDIO<15:4>	SDIO<3:0>
Product-ID<11:0> = 1F4 Hex	Die-Rev<3:0>

The Product ID = 1F4 Hex = 500 decimal.

Timing Protocol Diagram



Address Space

.

TABLE 74. Real Time DAC Storage

Register Bit	Central Bit	Channel Address						RT-DAC Bit	DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Static DC Level Storage																
0	0	0	0	0	0	0	0	0	F1	F0	0	0	0	0	0	I-Cl-Source
0	0	0	0	0	0	0	0	0	F1	F0	0	0	0	0	1	I-Cl-Sink
0	0	0	0	0	0	0	0	0	F1	F0	0	0	0	1	0	V-Cl-Hi
0	0	0	0	0	0	0	0	0	F1	F0	0	0	0	1	1	V-Cl-Lo
0	0	0	0	0	0	0	0	0	F1	F0	0	0	1	0	0	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	0	1	1	0	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	0	1	1	1	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	1	0	0	0	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	1	0	0	1	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	1	0	1	0	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	1	0	1	1	Not used
0	0	0	0	0	0	0	0	0	F1	F0	0	1	1	0	0	Not used
	•				•					•			•			Not used
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	Not used
Register Storage																
Register Bit	Central Bit	Channel Address						RT-DAC Bit	DAC Function		Resource Address					Description
1	X	0	0	0	0	0	0	X	A6	A5	A4	A3	A2	A1	A0	Registers

DC Level Function Decode							
F1	F0	A4	A3	A2	A1	A0	
0	0	X	X	X	X	X	DC Level
0	1	X	X	X	X	X	DC Level Offset
1	0	X	X	X	X	X	DC Level Gain
1	1	X	X	X	X	X	Not used

Registers

Control Registers																				
Register Big	Central Bit	RT-DAC Bit	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	0	0													WE	VCI<2>	VCI<1>	VCI<0>	Voltage Clamps
1	0	0	1			WE	Reserved	Sel-Diag<3>	Sel-Diag<2>	Sel-Diag<1>	Sel-Diag<0>	WE	Con-Cmin	WE	Con-CapB	Con-CapA	WE	Sel-MV<1>	Sel-MV<0>	Measurement Unit
1	0	0	2	WE	MI-OS<4>	MI-OS<3>	MI-OS<2>	MI-OS<1>	MI-OS<0>	WE	CMRR-Adj<4>	CMRR-Adj<3>	CMRR-Adj<2>	CMRR-Adj<1>	CMRR-Adj<0>	WE	IR<2>	IR<1>	IR<0>	CMRR Adjust/ Current Range Select/ MI Offset
1	0	0	3					WE	Con-Gang<3>	Con-Gang<2>	Con-Gang<1>	Con-Gang<0>	WE	Sel-Gang<1>	Sel-Gang<0>	WE	Sel-Force<2>	Sel-Force<1>	Sel-Force<0>	Forcing Voltage Control
1	0	0	4	Sel-V-FB<1>	Sel-V-FB<0>			WE	Sel-Mon-Ref	WE	CPU-Sel-FB<1>	CPU-Sel-FB<0>	WE	Sel-Ext-Mon-OE	WE	CPU-Mon-OE	WE	Sel-Mon<1>	Sel-Mon<0>	Monitor/Feedback Control
1	0	0	5	WE	Bypass-En	WE	DPS-En-Parity	WE	DPS-En-OE	WE	Sel-DPS-En	WE	CPU-En	WE	Sel-RT-En	WE	Local-Sense*	WE	FI/FV*	Mode Control/Chip Enable
1	0	0	6	WE	C-Bit	WE	Cap-Dis		WE	ES-OE	WE	Sel-ES<1>	Sel-ES<0>	WE	Sel-Con-FA-FB	WE	CPU-Con-FA-FB	WE	Con-EF-FB	Force/Sense Connections
1	0	0	7						WE	Sel-Adj<3>	Sel-Adj<2>	Sel-Adj<1>	Sel-Adj<0>	WE	Con-Cext	Con-Cint	WE	Reserved	Reserved	Slew Rate Control

Read Only

Resisters - continued

Register Big	Central Bit	RT-DAC Bit	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	0	64				WE	St-D14-Cal<4>	St-D14-Cal<3>	St-D14-Cal<2>	St-D14-Cal<1>	St-D14-Cal<0>	WE	St-D15-Cal<5>	St-D15-Cal<4>	St-D15-Cal<3>	St-D15-Cal<2>	St-D15-Cal<1>	St-D15-Cal<0>	Static DAC Cal Upper
1	0	0	65			WE	Reserved	WE	St-D11-Cal<1>	St-D11-Cal<0>	WE	St-D12-Cal<2>	St-D12-Cal<1>	St-D12-Cal<0>	WE	St-D13-Cal<3>	St-D13-Cal<2>	St-D13-Cal<1>	St-D13-Cal<0>	Static DAC Cal Middle Bits
1	0	0	66			WE	Sel-L-Icl-En	WE	I-Cl-En	WE	V-cl-En	WE	Sel-Global-Kel	CPU-Kel-En	WE	Kel-Al<3>	Kel-Al<2>	Kel-Al<1>	Kel-Al<0>	Kelvin Alarm/Clamps
1	0	0	67					WE	Sel-Global-OT	WE	Sel-tj-En	CPU-Tj-En	WE	CPU-OT-Flag-Dis	WE	Tj-Max<3>	Tj-Max<2>	Tj-Max<1>	Tj-Max<0>	Temperature Alarm
1	0	0	68	Global-Alarm	Kel-Al	OT-Flag	I-Cl	V-Cl		WE	Kel-Reset	WE	OT-Flat-Reset	WE	I-Cl-Reset	WE	CPU-OK-En	CPU-OT-Dis	CPU-OI-En	Alarm Control
1	0	0	69								WE	ED-Gain<7>	ED-Gain-<6>	ED-Gain<5>	ED-Gain<4>	ED-Gain<3>	ED-Gain<2>	ED-Gain<1>	ED-Gain<0>	External DAC
			70 - 127																	Not Used

Read Only

Write Only

Real Time DAC Registers

Register Big	Central Bit	RT-DAC Bit	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	1	0													WE	RTD<2>	RTD<1>	RTD<0>	RT DAC Range Selection
1	0	1	1	Start<15>	Start<14>	Start<13>	Start<12>	Start<11>	Start<10>	Start<9>	Start<8>	Start<7>	Start<6>	Start<5>	Start<4>	Start<3>	Start<2>	Start<1>	Start<0>	Adder Starting Address
1	0	1	2	Delta<15>	Delta<14>	Delta<13>	Delta<12>	Delta<11>	Delta<10>	Delta<9>	Delta<8>	Delta<7>	Delta<6>	Delta<5>	Delta<4>	Delta<3>	Delta<2>	Delta<1>	Delta<0>	Adder Increment Value
1	0	1	3		WE	Sel-Bin-Search	WE	Sel-Adder	WE	CPU-F-Sel	Sel-f-Sel	WE	CPU-Adder-CK	WE	Sel-Ext-Ld	Sel-Ext-U/D*	CPU-Ld	CPU-U/D*	Sel-Ext-Adder-Ck	Real Time Control
1	0	1	4	RT-Level<15>	RT-Level<14>	RT-Level<13>	RT-Level<12>	RT-Level<11>	RT-Level<10>	RT-Level<9>	RT-Level<8>	RT-Level<7>	RT-Level<6>	RT-Level<5>	RT-Level<4>	RT-Level<3>	RT-Level<2>	RT-Level<1>	RT-Level<0>	Real Time DAC Level
1	0	1	5	RT-Delta<15>	RT-Delta<14>	RT-Delta<13>	RT-Delta<12>	RT-Delta<11>	RT-Delta<10>	RT-Delta<9>	RT-Delta<8>	RT-Delta<7>	RT-Delta<6>	RT-Delta<5>	RT-Delta<4>	RT-Delta<3>	RT-Delta<2>	RT-Delta<1>	RT-Delta<0>	Real Time Delta
1	0	1	6	F0<15>	F0<14>	F0<13>	F0<12>	F0<11>	F0<10>	F0<9>	F0<8>	F0<7>	F0<6>	F0<5>	F0<4>	F0<3>	F0<2>	F0<1>	F0<0>	RT DAC Force 0 Value
1	0	1	7	F1<15>	F1<14>	F1<13>	F1<12>	F1<11>	F1<10>	F1<9>	F1<8>	F1<7>	F1<6>	F1<5>	F1<4>	F1<3>	F1<2>	F1<1>	F1<0>	RT DAC Force 1 Value

Read Only

Write Only

Real Time DAC Registers - continued

Register Big	Central Bit	RT-DAC Bit	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	1	8	F0-Offset<15>	F0-Offset<14>	F0-Offset<13>	F0-Offset<12>	F0-Offset<11>	F0-Offset<10>	F0-Offset<9>	F0-Offset<8>	F0-Offset<7>	F0-Offset<6>	F0-Offset<5>	F0-Offset<4>	F0-Offset<3>	F0-Offset<2>	F0-Offset<1>	F0-Offset<0>	RT DAC Force 0 Offset
1	0	1	9	F1-Offset<15>	F1-Offset<14>	F1-Offset<13>	F1-Offset<12>	F1-Offset<11>	F1-Offset<10>	F1-Offset<9>	F1-Offset<8>	F1-Offset<7>	F1-Offset<6>	F1-Offset<5>	F1-Offset<4>	F1-Offset<3>	F1-Offset<2>	F1-Offset<1>	F1-Offset<0>	RT DAC Force 1 Offset
1	0	1	10	F0=Gain<15>	F0=Gain<14>	F0=Gain<13>	F0=Gain<12>	F0=Gain<11>	F0=Gain<10>	F0=Gain<9>	F0=Gain<8>	F0=Gain<7>	F0=Gain<6>	F0=Gain<5>	F0=Gain<4>	F0=Gain<3>	F0=Gain<2>	F0=Gain<1>	F0=Gain<0>	RT DAC Force 0 Gain
1	0	1	11	F1=Gain<15>	F1=Gain<14>	F1=Gain<13>	F1=Gain<12>	F1=Gain<11>	F1=Gain<10>	F1=Gain<9>	F1=Gain<8>	F1=Gain<7>	F1=Gain<6>	F1=Gain<5>	F1=Gain<4>	F1=Gain<3>	F1=Gain<2>	F1=Gain<1>	F1=Gain<0>	RT DAC Force 1 Gain
1	0	1	12 - 64																	Not Used
1	0	1	64				WE	RT-D14-Cal<4>	RT-D14-Cal<3>	RT-D14-Cal<2>	RT-D14-Cal<1>	RT-D14-Cal<0>	WE	RT-D15-Cal<5>	RT-D15-Cal<4>	RT-D15-Cal<3>	RT-D15-Cal<2>	RT-D15-Cal<1>	RT-D15-Cal<0>	RT DAC Cal Upper Bits
1	0	1	65			WE	Reserved	WE	RT-D11-Cal>1>	RT-D11-Cal<0>	WE	RT-D12-Cal<2>	RT-D12-Cal<1>	RT-D12-Cal<0>	WE	RT-D15-Cal<3>	RT-D15-Cal<2>	RT-D15-Cal<1>	RT-D15-Cal<0>	RT DAC Force 0 Value
1	0	1	66 - 127																	Not Used

Central Registers

Register Big	Central Bit	RT-DAC Bit	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	0	0					WE	Reserved	Reserved	Reserved	WE	Reserved	WE	Reserved	Reserved	Reserved	Reserved	Reserved	Not Used
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU Reset
1	1	0	2												WE	Vmid<3>	Vmid<2>	Vmid<1>	Vmid<0>	Vmid
1	1	0	3 - 126																	Not used
1	1	0	127	Product-ID<11>	Product-ID<10>	Product-ID<9>	Product-ID<8>	Product-ID<7>	Product-ID<6>	Product-ID<5>	Product-ID<4>	Product-ID<3>	Product-ID<2>	Product_ID<1>	Product-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>	Die ID

Read Only

Write Only

Manufacturing Information

Moisture Sensitivity

Jupiter is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

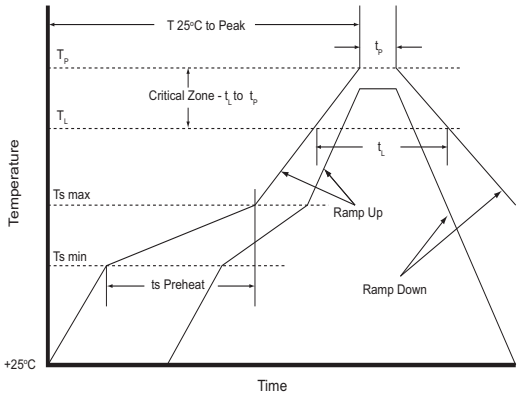
Chip Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead free or not.

PROFILE FEATURE	Pb-Free ASSEMBLY
Average ramp up rate (Ts max) to T_P)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 - 180 sec
ts max to T_p • Ramp Up Rate	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 217°C 60 - 150 sec
Peak Temperature (T_P)	250°C +0/–5°C
Time within 5°C of actual peak temp (tp)	20 to 40 sec
Ramp down rate	6°C/sec (max)
Time +25°C to peak temperature	8 minutes (max)



Thermal Analysis

JUNCTION TEMPERATURE

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$$Tj = Pd \bullet \theta JA + Ta$$

Tj = Junction Temperature

Pd = Power Dissipation

θJA = Thermal Resistance (Junction to Ambient)

Ta = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

CONDUCTION

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θJC) plus the resistance from the case to ambient (θCA)

CONVECTION

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

THERMAL RESISTANCE

Each system will have its own unique cooling strategy and overall θJA. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta JA = C + \theta CA$$

θCA is determined by the system environment of the part and is therefore application specific. θJC is determined by the construction of the part.

θJC Calculation

θJC = θ(silicon)

+ θ(die attach)

+ θ(paddle).

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistivity) • Thickness / Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

INTRINSIC THERMAL CONDUCTIVITY

Die Attach Thermal Conductivity = 1.4W/M°K

Silicon Thermal Conductivity = 141.2W/M°K

Paddle Thermal Conductivity = 263W/M°K

Plastic Thermal Conductivity = 0.88W/M°K

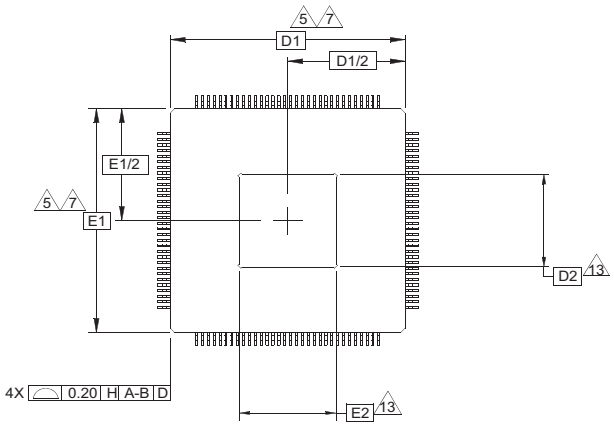
(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θJC through the paddle.

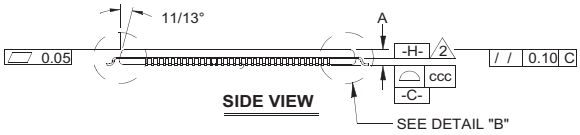
θJC = 0.11°C/W + .54°C/W + 0.01°C/W

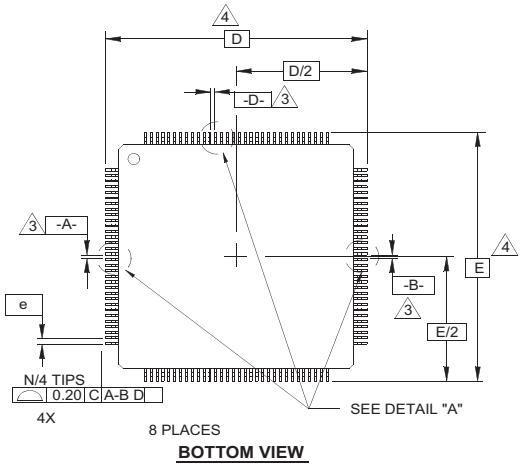
θJC = 0.66°C/W

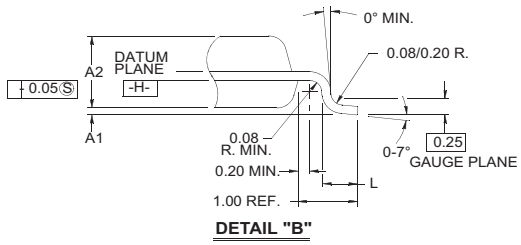
However, this calculation is based upon many ideal assumptions, and it should be treated as a best case value.

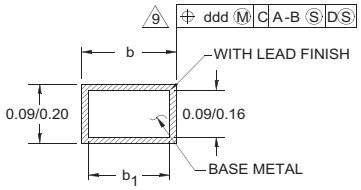
Package Outline Drawing











Q64.10x10E

64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE WITH TOP EXPOSED PAD (TEP-LQFP)

SYMBOL	ACD MIN	ACD NOM.	ACD MAX	NOTES
A			1.20	
A1	0.05		0.15	12
A2	0.95	1.00	1.05	
D		12.00 BSC		4
D1		10.00 BSC		7, 8
D2		7.49 BSC		13
E		12.00 BSC		4
E1		10.00 BSC		7, 8
E2		7.49 BSC		13
L	0.45	0.60	0.75	
N		64		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

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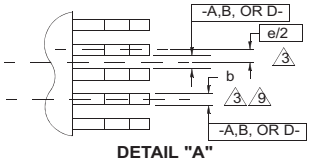
NOTES:

1. All dimensions and tolerances per ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at center line between leads where leads exit plastic body at datum plane -H- .
4. To be determined at seating plane -C- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. "N" is the total number of terminals.
7. These dimensions to be determined at datum plane -H- .
8. The top of package is smaller than the bottom of package by 0.15 millimeters.
9. Dimension b does not include dambar protrusion. allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. This outline conforms to jedec publication 95 registration MS-026, variations ACB, ACC, ACD & ACE.
12. A1 is defined as the distance from the seating plane to the lowest point of the package body.
13. Dimension D2 and E2 represent the size of the exposed pad.
14. Exposed pad shall be coplanar with bottom of package within 0.05.
15. JEDEC variation.



Revision History

Revision Date	Description of Changes
January 8, 2016	• Page 51: Power Supply Sequence Section - update power supply sequence
April 1, 2015	• Reformat from Intersil to Elevate Semiconductor format
October 16, 2013	• Page 45: Power Supplies: Add VCC_OUT - VEE (500mA Load) • Page 45: -Analog Pins - FORCE_B (active No Load) min rom VEE + 3 to VEE + 1 • Page 45: Add FORCE_B (Active 500mA Load) • Page 54: IR3, VR3 - change Imax to 512mA

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
Jupiter-314N	Jupiter-314N	+25 to +100	64 Lead, 10x10mm TQFP w/heat slug
Jupiter-314N-LB	Evaluation Board		
Jupiter-314N–SYS	Evaluation System		

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.