SOC Octal DPS/PMU/VI with Ganging 10MHz Pin Electronics

The Pluto2 is a highly integrated System-on-a-Chip (SOC) pin electronics solution incorporating 8 independent channels of:

- DPS/PMU/VI
- Pin Electronics
- Resistive Load

The interface, control, and the I/O are didital. All analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.

Features

- Per-Pin DPS/PMU
  - FV, FI, MV, MI - 4 Quadrant Operation
    - 64mA Imax in FV/MI
    - 32mA Imax in FI/MV
  - 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
  - 14V FV Range
  - FI Voltage Clamps
  - FV Current Clamps
  - Per Pin Monitor
  - Central (Per Chip) Monitor
- Pin Electronics Driver and Comparator
  - 2 Level Driver with On-Chip Buffers
  - 14V Driver Output Swings
  - 10MHz Driver Operation
  - 16V Comparator Input Voltage Range
  - Extremely Low Input Leakage over a 16V Range
- Ganging Capability
  - High Current Applications
  - No Limit on Ganged Imax
  - Gang Control Circuitry Built In
- 3 Bit Serial CPU Port
- On-Chip DAC to Generate DC Levels
  - 10 DC Levels per Channel (16 Bits/Level)
  - On-Chip Offset and Gain Correction
  - Ability to Shift Voltage Ranges Up and Down
- Package/Power Dissipation
  - Lead Free
  - 128 Lead, 14mm x 20mm TQFP with Heat Slug
  - Pdq 125mW/Channel; Pdq 1W/Chip
  - On-Chip Thermal Monitor

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers

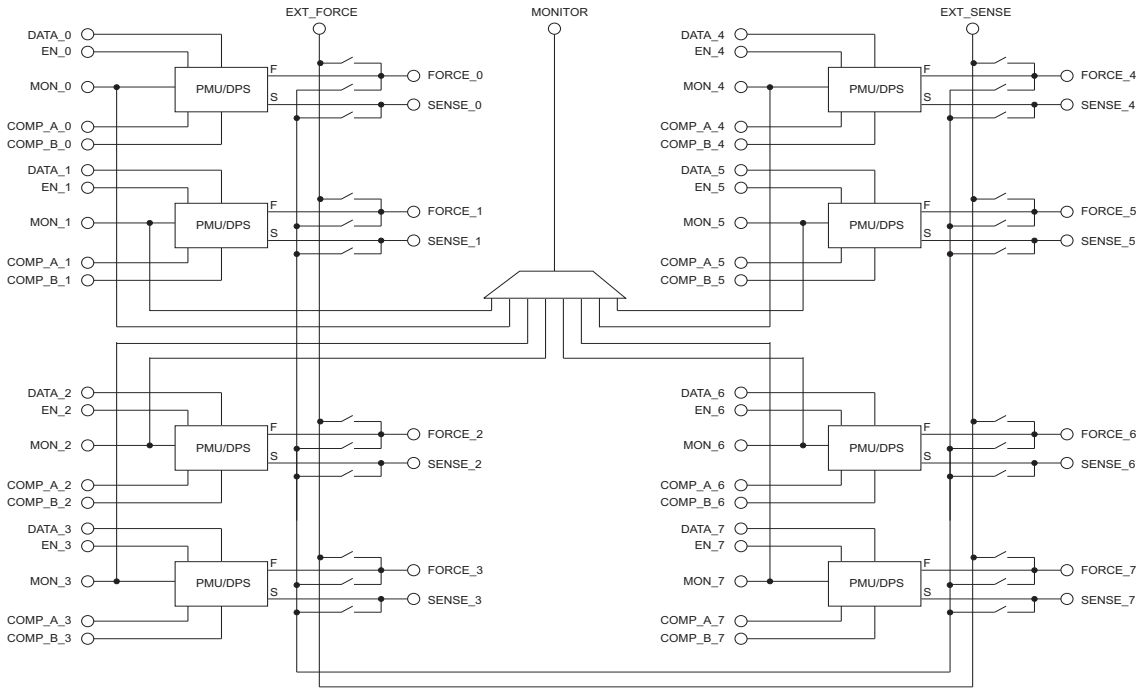


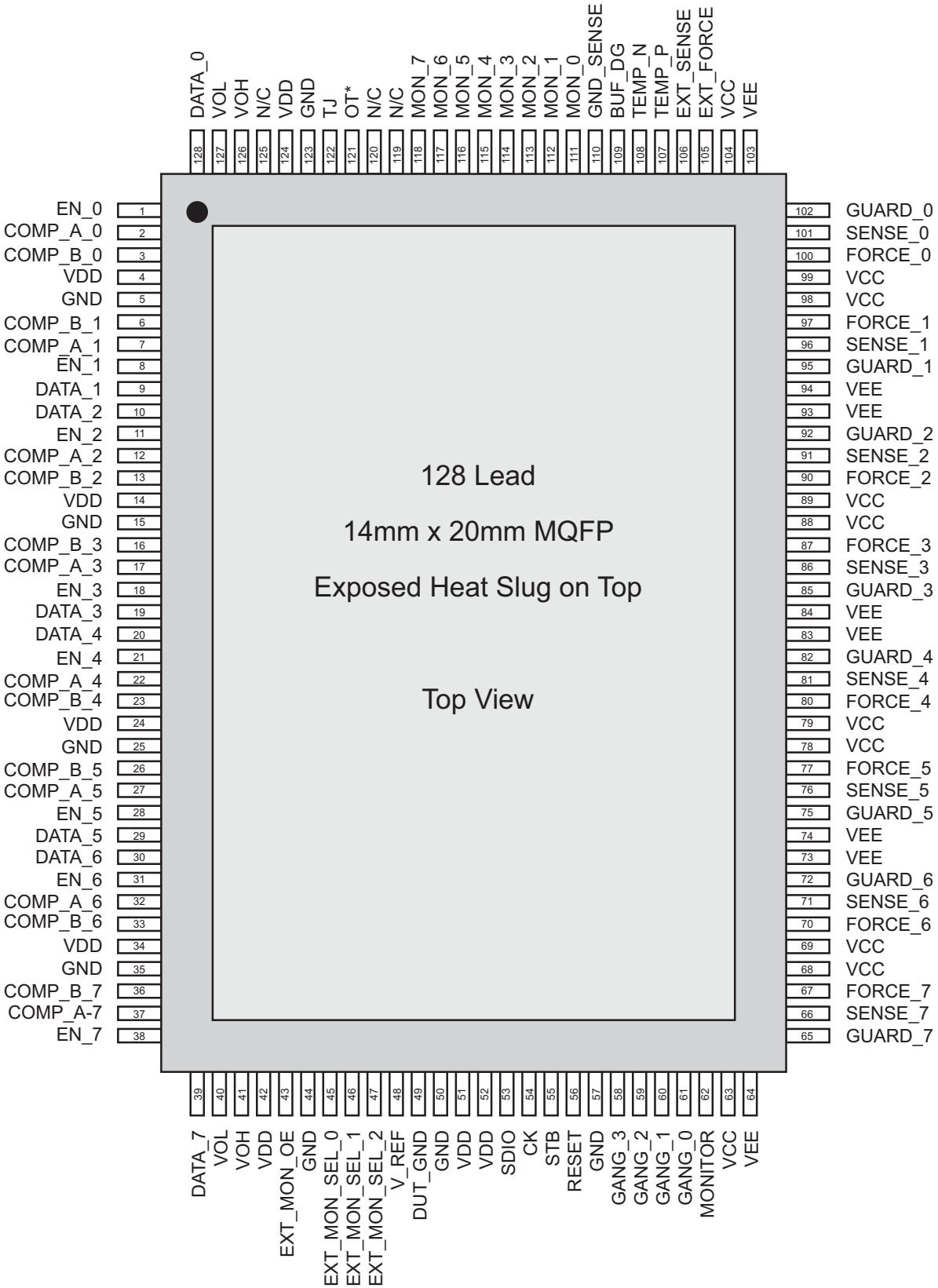
Table of Contents

PIn Descriptions

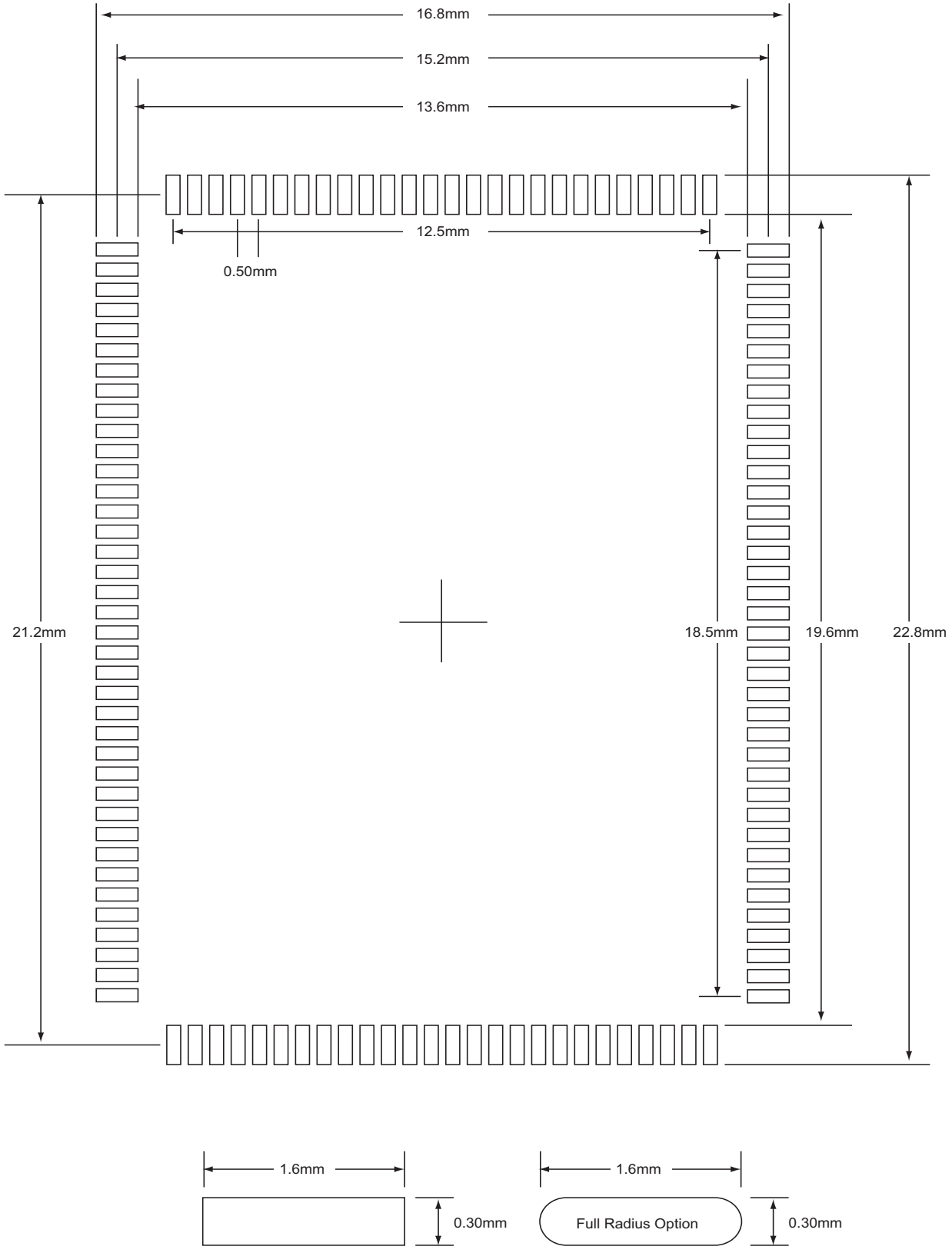
Pin Number	Pin Name	Description
100, 101, 102	FORCE_0, SENSE_0, GUARD_0	Channel 0 Force, Sense and Guard pins.
128, 1	DATA_0, EN_0	Channel 0 Driver Data and Enable inputs.
2, 3	COMP_A_0, COMP_B_0	Channel 0 Comparatour outputs.
97, 96, 95	FORCE_1, SENSE_1, GUARD_1	Channel 1 Force, Sense and Guard pins.
9, 8	DATA_1, EN_1	Channel 1 Driver Data and Enable inputs.
7,6	COMP_A_1, COMP_B_1	Channel 1 Comparatour outputs.
90, 91, 92	FORCE_2, SENSE_2, GUARD_2	Channel 2 Force, Sense and Guard pins.
10, 11	DATA_2, EN_2	Channel 2 Driver Data and Enable inputs.
12, 13	COMP_A_2, COMP_B_2	Channel 2 Comparator outputs.
87, 86, 85	FORCE_3, SENSE_3, GUARD_3	Channel 3 Force, Sense and Guard pins.
19, 18	DATA_3, EN_3	Channel 3 Driver Data and Enable inputs.
17, 16	COMP_A_3, COMP_B_3	Channel 3 Comparator outputs.
80, 81, 82	FORCE_4, SENSE_4, GUARD_4	Channel 4 Force, Sense and Guard pins.
20, 21	DATA_4, EN_4	Channel 4 Driver Data and Enable inputs.
22, 23	COMP_A_4, COMP_B_4	Channel 4 Comparator outputs.
77, 76, 75	FORCE_5, SENSE_5, GUARD_5	Channel 5 Force, Sense and Guard pins.
29, 28	DATA_5, EN_5	Channel 5 Driver Data and Enable inputs.
27, 26	COMP_A_5, COMP_B_5	Channel 5 Comparator outputs.
70, 71, 72	FORCE_6, SENSE_6, GUARD_6	Channel 6 Force, Sense and Guard pins.
30, 31	DATA_6, EN_6	Channel 6 Driver Data and Enable inputs.
32, 33	COMP_A_6, COMP_B_6	Channel 6 Comparator outputs.
67, 66, 65	FORCE_7, SENSE_7, GUARD_7	Channel 7 Force, Sense and Guard pins.
39, 38	DATA_7, EN_7	Channel 7 Driver Data and Enable inputs.
37, 36	COMP_A_7, COMP_B_7	Channel 7 Comparator outputs.
Central Resource Pins		
48	V_REF	External precision voltage reference.
49	DUT_GND	Analog voltage input used to track ground at the DUT.
61, 60, 59, 58	GANG_0, GANG_1, GANG_2, GANG_3	Analog voltage I/O pins used for current ganging.
105, 106	EXT_FORCE, EXT_SENSE	External PMU connection pins.
110	GND_SENSE	Ground sense point.
109	BUF_DG	Buffered DUT Ground output.
108, 107	TEMP_N, TEMP_P	Terminals of an on-chip thermal diode.
122	TJ	Analog voltage output that tracks junction temperature.
121	OT*	Over temperature open drain digital output.
62	MONITOR	Analog voltage output of the PPMU

Pin Number	Pin Name	Description
CPU Interface		
54, 53, 55	CK, DKIO, STB	3-bit serial port (Clock, Data and Strobe).
57	RESET	Chip reset.
External Monitor Control		
43	EXT-MON_OE	External Monitor output enable control.
45, 46, 47	EXT_MON_SEL<0:2>	External Monitor selection control bits.
111, 112, 113, 114	MON_<0:3>	External per channel Monitor outputs.
115, 116, 117, 118	MON_<4:7>	External per channel Monitor outputs.
Power Supplies		
63, 68, 69, 79, 88, 89, 98, 99, 104	VCC	Analog positive power supply.
64, 73, 74, 83, 84, 93, 94, 103	VEE	Analog negative voltage supply.
4, 14, 24, 34, 42, 51, 52, 124	VDD	Digital power supply.
5, 15, 25, 35, 44, 50, 57, 123	GND	Digital ground.
41, 126	VOH	Comparator output high level power supply.
40, 127	VOL	Comparator output low level power supply.

Pin Configuration



Recommended PCB Footprint



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	VDD		+18	V
VEE	–4		0	V
VCC – VEE	0		+18	V
VDD	0		+5	V
VDD – VEE	0		+7.5	V
VOH			VDD + 0.9	V
VOL	GND – 0.9			V
Analog Input/Output Voltages				
FORCE, SENSE, GUARD	VEE –0.9		VCC + 0.9	V
EXT_SENSE	VEE –0.9		VCC + 0.9	V
EXT_FORCE	VEE – 0.9		VCC + 0.9	V
TJ	GND – 0.9		VDD + 0.9	V
Digital Output Currents/Voltages				
COMP_A, COMP_B	–80		80	mA
SDIO	–20		20	mA
OT*	GND – 0.9		VDD + 0.9	V
OT* Iout			20	mA
External References				
V_REF	GND – 0.9		VDD + 0.9	V
Temperature				
Junction Temperature	–55		150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+6	+12.5	+14	V
VEE	–3.7	–3.5	–2.7	V
VDD	+3.25	+3.3	+3.45	V
GND		0		V
VCC – VEE		+16	+17	V
VDD – VEE		+6.3	+7.0	V
Comparator Output Supplies				
VOH			VCC	V
VOL	GND			V
VOH – VOL	0.4		VDD –GND	V
PMU Levels				
V-FV (No Load)	VEE + 1		VCC – 1	V
V-FV (Maximum Load) (IR0 – IR5)	VEE + 2		VCC – 2	V
V-FV (Maximum Load) (IR6 – IR7)	VEE + 3		VCC – 3	V
MV @ Monitor	VEE + 2.5		VCC – 1	V
FORCE/SENSE Input Compliance	VEE		VCC	V
Digital Pins				
SK, SDIO, STB, RESET	GND		VCC	V
Driver Levels				
VTT	VEE + 1		VCC – 1	V
DVL	VEE + 1		VCC – 1	V
Threshold Levels				
CVA_PPMU, CVB_PPMU	VEE + 1		VCC – 1	V
Clamp Levels				
V-Cl-Hi	VEE + 3		VCC – 1	V
V-Cl-Lo	VEE + 2		VCC – 3	V
V-Cl-Hi – V-Cl-Lo	1			V
I, Cl-Hi, I-Cl-Lo	–150%		+300%	Imax
SENSE (w/voltage clamps active)	VCL + 100mV		VCC – 100mV	V
MI (w/current clamps active)	.01 • ICL		.99 • ICH	mA
External References				
V_REF	+2.99	+3.0	+3.01	V
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V

Recommended Operating Conditions - cont'd

Parameter	Min	Typ	Max	Units
Capacitive Load (Con-Cext# = 0)				
IR7			400	nF
IR6			100	nF
IR5			40	nF
IR4			10	nF
IR3			4	nF
IR2			2	nF
IR1			1	nF
IR0			1	nF
Capacitive Load (Con-Cext# = 1, in DPS Mode)				
IR7			2	µF
IR6			500	nF
IR5			200	nF
IR4			50	nF
IR3			20	nF
IR2			10	nF
IR1			5	nF
IR0			5	nF
Miscellaneous				
Junction Temperature	25		100	°C
TJ	GND		VDD	V
OT*	GND		VDD	V
OT* Iout			10	mA
CPU Port CK Frequency	10		25	MHz

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Characteristics - Power Supply Current

VCC = +2.75V, VEE = –3.7V, VDD = +3.5V, V_REF = 3.00V, DUT_GND = 0V unless otherwise specified. The total chip power values are based upon typical supply currents and nominal supply levels.

Spec #	Parameter	Conditions	Min	Typ	Max	Units	Pd (Typ)
No Load							
11100	ICC	Note 1	40	55	70	mA	688mW
11200	IEE	Note 1	45	60	75	mA	210mW
11300	IDD	Note 1	30	45	60	mA	149mW
							1.0W/Chip
Sourcing 32mA Load/Channel							
11110	ICC	Notes 2, 4	300	325	350	mA	4,063mW
11120	IEE	Notes 2, 4	55	70	85	mA	245mW
11130	IDD	Notes 2, 4	55	70	85	mA	231mW
							4.5W/Chip
Sinking 32mA Load/Channel							
11140	ICC	Notes 3, 4	45	65	80	mA	813mW
11150	IEE	Notes 3, 4	305	330	355	mA	1150mW
11160	IDD	Notes 3, 4	55	70	85	mA	231mW
							2.2W/Chip

Notes:

1. All 8 channels in FV, MI mode. V_FV = +3V; Iout = 0mA.
2. V_FV = +3V; Iout = +32mA per channel (sourcing current).
3. V_FV = +3V; Iout = –32mA per channel (sinking current).
4. Channel 0 in FV mode (master). Channels 1-7 in FI mode (slave). All channels ganged together.

DC Characteristics - Thermal Monitor and Alarm

VCC = +2.5V, VEE = –3.5V, VDD = +3.3V, V_REF = 3.00V, DUT_GND = 0V unless otherwise specified.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
TJ, OT*						
10096	TJ HiZ Leakage	Tested at 0V and VDD	–5	0	+5	nA
10095	Over Temperature Threshold		120	135	150	°C
10094	OT* VOH (HiZ Leakage)	Tested at 0V and VDD	–5	0	+5	nA
10093	OT* VOL	Input current = 4mA			.4	V

DC Characteristics - CPU Port

Spec #	Parameter	Conditions	Min	Typ	Max	Units
SDIO, CK, STB, RESET						
17100	VIH	Note 5	2.0			V
17110	VIL	Note 5			0.8	V
17120	Iin (Input Leakage Current)	Tested at VDD; Note 6	–100	0	+100	nA
17200	VOH (SDIO only)	Note 5, 7	2.4			V
17210	VOL (SDIO only)	Notes 5, 8			0.8	V

DC Characteristics - Digital Inputs/Outputs

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Comparator Outputs (COMP_A, COMP_B)						
13361	VOH Output Impedance	Note 5	30	50	75	Ω
13360	VOL Output Impedance	Note 5	30	50	75	Ω
DATA, EN, EXT_MON_OE, EXT_MON_SEL<2:0> Inputs						
13260	VIH	Note 5	2.0			V
13261	VIL	Note 5			0.8	V
13262	Iin (Input Leakage Current) (HiZ)	Tested at VDD; Note 6	–100	0	+100	nA

NOTES:

5. VCC = +12.5V, VEE = –3.5V, VDD = +3.3V, V_REF = 3.00V, DUT_GND = 0.
6. VCC = +12.75V, VEE = –3.7V, VDD = +3.5V, V_REF = 3.00V, DUT_GND = 0.
7. Output Current = 2mA (sourcing).
8. Output Current = 2mA (sinking).

DC Characteristics - Analog Pins

Spec #	Parameter	Conditions	Min	Typ	Max	Units
10999	V_REF Input Current	Note 9	–1	0	+1	µA
10998	DUT_GND Input Current	Tested at 0V; Note 9	–15	0	+15	nA
14090	GUARD_#, FORCE_#, SENSE_# HiZ Leakage	Tested at 0V; Note 9	–10	0	+10	nA
14091	GUARD_#, FORCE_#, SENSE_# HiZ Leakage	Tested at VCC, VEE; Note 9	–15	0	+15	nA
10997	EXT_FORCE, EXT_SENSE HiZ Leakage	Tested at 0V; Note 9	–10	0	+10	nA
10996	EXT_FORCE, EXT_SENSE HiZ Leakage	Tested at VCC, VEE; Note 9	–15	0	+15	nA
14092	GANG_0-3 HiZ Leakage	Tested at 0V; Note 9	–10	0	+10	nA
14093	GANG_0-3 HiZ Leakage	Tested at VCC, VEE; Note 9	–15	0	+15	nA
	FORCE_# Capacitance	Note 10		9		pF
	SENSE_# Capacitance	Note 10		5		pF
	EXT_FORCE Capacitance	Note 10		25		pF
	EXT_SENSE Capacitance	Note 10		8		pF

NOTES:

9. VCC = +12.75V, VEE = –3.7V, VDD = +3.5V, V_REF = 3.00V, DUT_GND = 0.
10. Limits established by characterization and are not production tested.

DC Characteristics - Level DAC Calibration

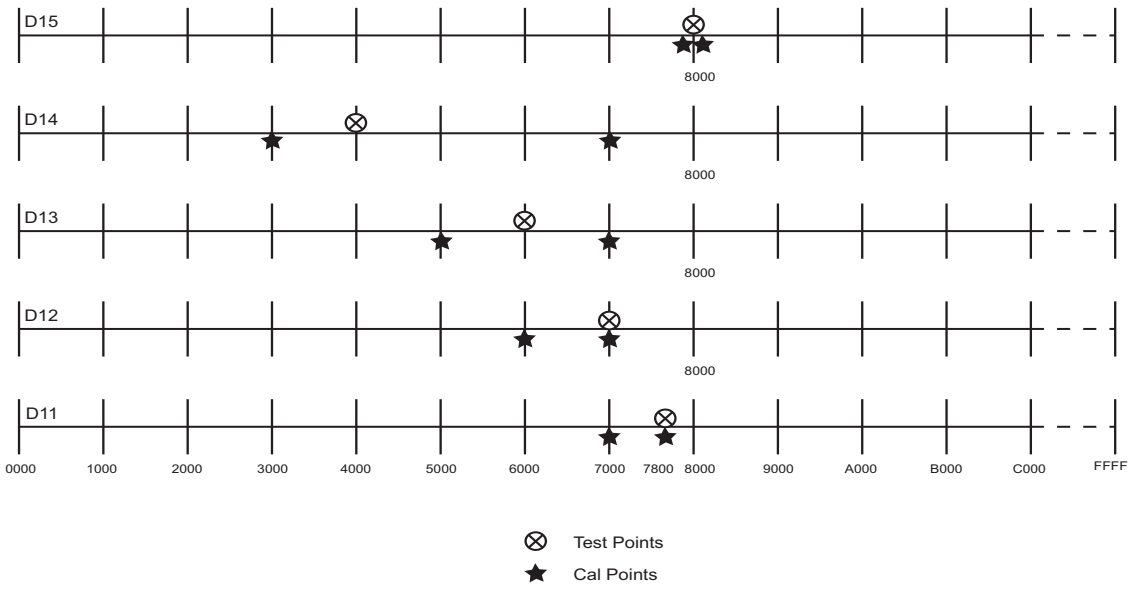
All DC tests are performed after the DAC is first calibrated. The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carries as small as possible.

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
16510	Level DAC D15 Step Error	Code 8000 – Code 7FFF – LSB; VR1; Note 11	–5		+5	mV
16520	level DAC D14 Step Error	Code 4000 – Code 3FFF – LSB; VR1; Note 12	–5		+5	mV
16530	Level DAC D13 Step Error	Code 6000 – Code 5FFF –LSB; VR1; Note 13	–5		+5	mV
16540	Level DAC D12 Step Error	Code 7000 – Code 6FFF – LSB; VR1; Note 14	–5		+5	mV
16550	Level DAC D11 Step Error	Code 7800 – Code 77FF – LSB ; VR1; Note 15	–5		+5	mV

NOTES:

11. (DAC @ 8000 – DAC @ 7FFF) / (8000 –7FFF) – DAC LSB; VR1
12. (DAC @ 7000 – DAC @ 3000) / (7000 – 3000) – DAC LSB; VR1
13. (DAC @ 7000 – DAC @ 5000) / (7000 – 5000) – DAC LSB; VR1
14. (DAC @ 7000 – DAC @ 6000) / (7000 – 6000) – DAC LSB; VR1
15. (DAC @ 7800 – DAC @ 7000) / (7800 – 7000) – DAC LSB; VR1



DC Characteristics - DAC

There are 3 on-chip internal DACs per channel used for:

1. DC Level
2. DC Level Offset Correction
3. DC Level Gain Correction

DAC testing is performed post DAC Calibration. These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator, and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Level DAC Test						
16100	Span	Span = DAC(FFFF) – DAC(0000); Notes 16, 17	7.6	8.2	8.6	V
16110	Linearity Error	Notes 16, 17, 18	–7.5	0	+7.5	mV
16120	Bit Test Error	Notes 16, 17, 19	–7.5	0	+7.5	mV
16190	Droop Test	Note 20	–300		+300	µV/ms
16400	DAC Noise	FV = 0V, VR2, measured at FORCE_0, RMS measurement			+1.0	mV
Offset DAC Test						
16200	+Adjustment Range	Level and Gain DACs both programmed to midscale (Code 7FFF); Notes 16, 21	+4.5	+5.4	+6.0	% of Span
16210	–Adjustment Range	Level and Gain DACs both programmed to midscale (Code 7FFF); Notes 16, 21	–6.0	–5.4	–4.5	% of Span
16220	Linearity Error	Level and Gain DACs both programmed to midscale (Code 7FFF); Notes 16, 18	–5	0	+5	mV
16230	Bit Test Error	Level and Gain DACs both programmed to midscale (Code 7FFF); Notes 16, 19	–5	0	+5	mV
Gain DAC Test						
16300	+Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF; Note 16	1.1	1.125	1.15	V/V
16310	–Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF; Note 16	.850	.875	.90	V/V
16320	Linearity Error	Level DAC = FFFF, Offset DAC = 7FFF; Notes 16, 18	–3	0	+3	mV/V
16330	Bit Test Error	Level DAC = FFFF, Offset DAC = 7FFF; Notes 16, 19	–3	0	+3	mV/V

NOTES:

16. DAC tests performed using the PMU in FV mode and the MONITOR output VR1.
17. Offset and Gain DACs both programmed to midscale (Code 7FFF).
18. Linearity Test - 17 equal spaced codes relative to a straight line determined by 1/8 and 7/8 measurement points: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF.
19. Bit Test - Walking 1 and Walking 0 to determine the correct bit weight:
    1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0800, 0040, 0020, 0010, 0008, 0004, 0002, 0001
    0's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
20. CPU CK turned off. 66ms delay between measurements. Each DC level on the chip checked on at a time.
21. Code 0000, FFFF relative to midscale (7FFF).

DC Characteristics - Vmid DAC

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V. DAC tests performed in FV mode tested at the MONITOR.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Vmid Shift in VR0						
16400	Code 01 vs. Code 00	CODE1, Note 22	+0.2	+0.25	+0.3	V
16400	Code 10 vs. Code 00	CODE2, Note 22	–0.3	–0.25	–0.2	V
16400	Code 11 vs. Code 00	CODE3, Note 22	–0.55	–0.5	–0.45	V
Vmid Shift in VR1						
16400	Code 01 vs. Code 00	CODE1, Note 23	+0.4	+0.5	+0.6	V
16400	Code 10 vs. Code 00	CODE2, Note 23	–0.6	–0.5	–0.4	V
16400	Code 11 vs. Code 00	CODE3, Note 23	–1.1	–1.0	–0.9	V
Vmid Shift in VR2						
16400	Code 01 vs. Code 00	CODE1, Note 24	+0.85	+1.0	+1.15	V
16400	Code 10 vs. Code 00	CODE2, Note 24	–1.15	–1.0	–0.85	V
16400	Code 11 vs. Code 00	CODE3, Note 24	–2.15	–2.0	–1.85	V

NOTES:

22. VR0, tested with DAC programmed to –0.5V and +3.5V with Vmid<1:0> = 00 as reference voltage.
23. VR1, tested with DAC programmed to –1V and +7V with Vmid<1:0> = 00 as reference voltage.
24. VR2, tested with DAC programmed to 0V and +10V with Vmid<1:0> = 00 as reference voltage.

DC Characteristics - Force Voltage

The sequence of events performed for FV testing is:

1. Program FV
2. Force current at FORCE
3. Measure the voltage at FORCE

FV Tests:

1. VR0 tested in IR5
2. VR1 tested in IR5
3. VR2 tested in all current ranges

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
FV Post Calibration						
14200	Output Force Error	VR0, Cal0, FV VR0 Test Points	–4		+4	mV
14201	Output Force Error	VR1, Cal1, FV VR1 Test Points	–7.5		+7.5	mV
14202	Output Force Error	VR2, Cal2, FV VR2 Test Points	–15		+15	mV
14208	Short Circuit Output Current (Source)	Note 25	150	180	250	mA
14209	Short Circuit Output Current (Sink)	Note 26	–250	–225	–150	mA
	FV Temperature Coefficient	VR1, Note 27		<–50		µV/ °C

NOTES:
25. VR2, IR7, FORCE = +10V, Vload = 0V, Remote Sense
26. VR2, IR7, FORCE = 0V, Vload = +10V, Remote Sense
27. Guaranteed by characterization. Not production tested.

TABLE 1.

FV		
Range	**Cal Points**	**FV Test Points**
VR0 IR5	0V/0µA +3V/0µA	–5V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR5	0V/0µA +5V/0µA	–1V/0µA +3V/0µA +7V/0µA
VR2 IR5	0V/0µA +8V/0µA	–2V/0µA +11.5V/0µA
VR2 IR0 - IR5	0V/0µA +8V/0µA	–1.5V/0µA +11V/0µA
VR2 IR6 - IR7	0V/0µA +8V/0µA	–1V/0µA +9.5V/0µA

DC Characteristics - Measure Current

MI tested in VR2, IR0 - IR7. VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
MI (Post Calibration)						
14100	Measure Current Error	TPMI-A, IR0, Note 28	–6		+6	nA
14101	Measure Current Error	TPMI-A, IR1, Note 28	–24		+24	nA
14102	Measure Current Error	TPMI-A, IR2,Note 28	–96		+96	nA
14103	Measure Current Error	TPMI-A, IR3, Note 28	–384		+384	nA
14104	Measure Current Error	TPMI-A, IR4, Note 28	–1.536		+1.536	µA
14105	Measure Current Error	TPMI-A, IR5, Note 28	–6		+6	µA
14106	Measure Current Error	TPMI-B, IR6, Note 28	–24		+24	µA
14107	Measure Current Error	TPMI-B, IR7, Note 28	–96		+96	µA
14117	Measure Current Error	TPMI-C, IR7, Note 28	–200		+200	µA
14127	Measure Current Error	TPMI-D, IR7, Note 28	–2		+2	mA
	MI Temperature Coefficient	IR2; Note 29		<+1		nA/°C
	MI Temperature Coefficient	IR5; Note 29		<+125		nA/°C
	MI Temperature Coefficient	IR7, Note 29		<+2.5		µA/°C

NOTES:
28. 4-point software calibration for MI CMRR and a 2-point MI calibration.
29. Limits established by characterization and are not production tested.

TABLE 2.

Range	Cal Points	TPMI-A	TPMI-B	TPMI-C	TPMI-D
IR0 - IR5	+4V/+0.8 • Imax +4V/ –0.8 • Imax	–2V/0µA +11V/0µA –1.5V/–Imax +11V/+Imax			
IR6, IR7	+4V/+0.8 • Imax +4V/ –0.8 • Imax		–2V/0µA +11V/0µA –0.5V/–Imax +9.5V/+Imax		
IR7				+4V/ +2 • Imax	
IR7					+4V/ –2 • Imax

DC Characteristics - Force Current

The sequence of events performed for FI testing is:

1. Program FI to the desired current
2. Force voltage with external PMU at FORCE
3. Measure the current at FORCE

FI is tested in all 8 current ranges.

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Post Calibration FI Error						
14800	Force Current Error	TPFI-A, IR0	–10		+10	nA
14801	Force Current Error	TPFI-A, IR1	–40		+40	nA
14802	Force Current Error	TPFI-A, IR2	–160		+160	nA
14803	Force Current Error	TPFI-A, IR3	–0.64		+0.64	µA
14804	Force Current Error	TPFI-A, IR4	–2.56		+2.56	µA
14805	Force Current Error	TPFI-A, IR5	–10		+10	µA
14806	Force Current Error	TPFI-B, IR6	–40		+40	µA
14807	Force Current Error	TPFI-B, IR7	–160		+160	µA
	FI Temperature Coefficient	IR2; Note 30		<+4		nA/°C
	FI Temperature Coefficient	IR5; Note 30		<+250		nA/°C
	FI Temperature Coefficient	IR7, Note 30		<+5		µA/°C
Pre-Calibration CMRR						
14203	IR0	Note 31	–7.5		+7.5	nA/V
14213	IR1	Note 31	–30		+30	nA/V
14223	IR2	Note 31	–120		+120	nA/V
14233	IR3	Note 31	–480		+480	nA/V
14243	IR4	Note 31	–1.92		+1.92	µA/V
14253	IR5	Note 31	–7.5		+7.5	µA/V
14263	IR6	Note 31	–30		+30	µA/V
14273	IR7	Note 31	–120		+120	µA/V

NOTES:

30. Limits established by characterization and are not production tested.
31. VR2, Loop# = 1, FI = 0mA.

FI Testing	Cal Points	TPFI-A	TPFI-B
IR0 - IR5	+4V/+0.8 • Imax +4V/ –0.8 • Imax	–1.5V/0µA +11V/0µA –1V/–Imax +11V/+Imax	
IR6 - IR7	+4V/+0.8 • Imax +4V/ –0.8 • Imax		–1.5V/0µA +11V/0µA –0.5V/–Imax +9V/+Imax

DC Characteristics – Measure Voltage (Monitor)

The sequence of events performed for testing the MONITOR is:

1. Program FV to the desired voltage (in VR2, IR5, Iload = 0)
2. Measure the voltage at FORCE
3. Measure the voltage at MONITOR
4. Calculate the difference to determine the error.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Central Monitor						
14710	HiZ Leakage Current	Notes 32, 34	–5	0	+5	nA
19100	Central MONITOR Output Impedance	Notes 32, 35	0.75	1.1	1.75	KΩ
14720	Voltage Error	MV Test Points; Note 33	–5	0	+5	mV
	Monitor Temperature Coefficient	Notes 33, 38		<+50		µA/°C
Per Channel Monitor						
19112	Per Channel MON_# Output Impedance	Notes 32, 35		250	500	Ω
14721	Per Channel MON_# Voltage Error	Note 33	–5		+5	mV
19114	BUF_DG Output Impedance	Notes 32, 35	1	1.25	1.5	KΩ
14741	DUT_GND Error	Notes 33, 37	–5		+5	mV
19113	GND_SENSE Output Impedance	Notes 32, 35	400	750	1,250	Ω

NOTES:

32. VCC = +12.5V, VEE = –3.5V, VDD = +3.5V, V_REF = 3.00V, DUT_GND = 0V.
33. VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.
34. Tested at MONITOR = 0V, VCC, VEE
35. Tested at +4V, Iout = 0µA/+100µA and 0µA/–100µA.
36. DUT_GND = ±300mV, Mon-GND-OE = 1; Measured at EXT_SENSE relative to GND, Post Cal.
37. DUT_GND = ±300mV, FV Mode, V-FV = +3.0V; Measured at FORCE relative to GND.
38. Guaranteed by characterization. Not production tested.

DC Characteristics - Measure Voltage (Comparator)

The window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Central Monitor						
14600	Threshold Error, VR0	Cal0, Note 39	–4		+4	mV
14601	Threshold Error, VR1	Cal1, Note 40	–7.5		7.5	mV
14602	Threshold Error, VR2	Cal2, Note 41	–15		+15	mV
14603	Threshold Error, VIR	Cal3, Note 42	–4		+4	mV
	Comparator Threshold Tempco	VR2, Note 43		<+200		µV/°C

NOTES:

39. PMU comparator threshold test points, VR0, test the internal references via Test & Cal Mux.
40. PMU comparator threshold test points, VR1, test the internal references via Test & Cal Mux.
41. PMU comparator threshold test points, VR2, test the comparator outputs using a binary search.
42. PMU comparator threshold test points, VIR, test the internal references via Test & Cal Mux.
43. Guaranteed by characterization. Not production tested.

TABLE 3.

Range	Cal Points	Test Points
VR0	0V +3V	–0.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +8V	–2V +6V +10V
VIR	–0.8V +0.8V	–1V 0V +1V

DC Characteristics - Driver

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
DVL/VTT						
12100	Driver Output Error, VR0	Notes 44, 45	–4		+4	mV
12110	Driver Output Error, VR1	Notes 44, 46	–7.5		+7.5	mV
12120	Driver Output Error, VR2	Notes 44, 47	–15		+15	mV
12130	Driver Output Error, VIR	Notes 44, 47	–4		+4	mV
	Temperature Coefficient	VR2, Note 49		–150		µV/°C

NOTES:
44. DVL–# or VTT–# as forcing voltage, measured at FORCE_#.
45. Fast driver mode test and cal points, VR0.
46. Fast driver mode test and cal points, VR1.
47. Fast driver mode test and cal points, VR2.
48. Fast driver mode test and cal points, VIR.
49. Limits established by characterization and are not production tested.

TABLE 4.

Range	Cal Points	Test Points
VR0	0V +3V	–0.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +8V	–1V +6V +9V
VIR	–0.8V +0.8V	–1V 0V +1V

DC Characteristics - Voltage Clamp Low

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
14400	Low Voltage Clamp Error, VR0	Low voltage clamp test points, VR0.	–10		+10	mV
14410	Low Voltage Clamp Error, VR1	Low voltage clamp test points, VR1.	–15		+15	mV
14420	Low Voltage Clamp Error, VR2	Low voltage clamp test points, VR2.	–20		+20	mV
	Low Voltage Clamp Tempco	Note 50		<–1.5		mV/°C

NOTES:
50. Limits established by characterization and are not production tested.

TABLE 5.

Range	Cal Points	Test Points
VR0	0V +3V	–0.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +6V	–1V +3V +7V

DC Characteristics - Voltage Clamp High

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
14440	High Voltage Clamp Error, VR0	High voltage clamp test points, VR0.	–10		+10	mV
14450	High Voltage Clamp Error, VR1	High voltage clamp test points, VR1.	–15		+15	mV
14460	High Voltage Clamp Error, VR2	High voltage clamp test points, VR2.	–20		+20	mV
	High Voltage Clamp Tempco	Note 51		<4		mV/°C

NOTES:
51. Limits established by characterization and are not production tested.

TABLE 6.

Range	Cal Points	Test Points
VR0	+1V +3V	+1V +1.5V +3.5V
VR1	+1V +5V	+1V +3V +7V
VR2	+1V +10V	+1V +5V +11V

DC Characteristics - Current Clamps

Current clamps are tested in all 8 current ranges. The sequence of events to test the high current clamps are:

1. Program I-Cl-Hi
2. Program FV = +4V
3. Program the tester PMU to +3V
4. Measure the current at FORCE

The sequence of events to test the low current clamps is:

1. Program I-Cl-Lo
2. Program FV = +4V
3. Program the tester PMU to +5V
4. Measure the current at FORCE

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
	High Current Clamp Tempco	IR0 - IR7, Note 52		0.1		%FS/°C
	Low Current Clamp Tempco	IR0 - IR7, Note 52		0.1		%FS/°C
13500	High/Low Current Clamp Error	IR0	–2		+2	%FS
13501	High/Low Current Clamp Error	IR1	–1.5		+1.5	%FS
13502	High/Low Current Clamp Error	IR2	–1		+1	%FS
13503	High/Low Current Clamp Error	IR3	–1		+1	%FS
13504	High/Low Current Clamp Error	IR4	–1		+1	%FS
13505	High/Low Current Clamp Error	IR5	–1		+1	%FS
13506	High/Low Current Clamp Error	IR6	–1		+1	%FS
13507	High/Low Current Clamp Error	IR7	–1		+1	%FS

FS: Full Scale = 3 • Imax

NOTES:

52. Limits established by characterization and are not production tested.

TABLE 7.

Range	Cal Points	Test Points
I-Cl-Hi	0µA +2 • Imax	–0.5 • Imax –1.5 • Imax +3.0 • Imax
I-Cl-Lo	–0.8 • Imax +0.8 • Imax	–1.0 • Imax 0 +1.0 • Imax

DC Characteristics - Resistance Values

VCC = +12.5V, VEE = –3.5V, VDD = +3.3V, V_REF = 3.00V, DUT_GND = 0V.

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Sense Resistors						
19000	IR0	Note 53		500		KΩ
19010	IR1	Note 53		125		KΩ
19020	IR2	Note 53		31.25		KΩ
19030	IR3	Note 53		7.81		KΩ
19040	IR4	Note 53		1.95		KΩ
19050	IR5	Note 53		500		Ω
19060	IR6	Note 53		125		Ω
19070	IR7	Note 53		31.25		Ω
On-Chip FET Switches						
19102	PPMU#-Con		10	17	25	Ω
19103	Con-FS		1.5	3	5	KΩ
19106	Con-ES-S#		1.5	3	5	KΩ
19104	RT-Con-EF#		15	25	35	Ω
19105	Con-ES-F#		1.5	3	5	KΩ
19116	Con-Cext#		15	25	35	Ω
19117	Guard-En#		1.5	3	5	KΩ
19101	GND_OE		8	11	15	KΩ
19115	SENSE#_DIS		1.5	3	5	KΩ
19118	Connect Diode	Note 54	50	70	90	Ω
Ganging Switches						
19107	Con-Int-Gang		4	6	9	KΩ
10108	Con-Ext-Gang		4	6	9	KΩ
Output Impedances						
19109	DVL Driver Output Impedance		25	35	45	Ω
19111	HiZ Force Output Impedance		.75	1.5	1.75	KΩ

NOTES:

53. Measured via monitor, therefore, appears 2 times actual value.
54. Diode connect switch plus the diode on resistance.

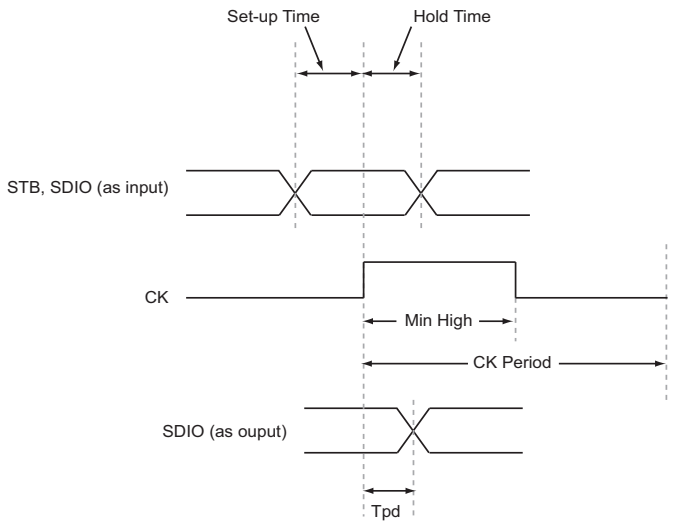
AC Characteristics

NOTE: For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Characteristics - CPU Port

VCC = +12.25V, VEE = –3.4V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V. Limits established by characterization and are not production tested..

Spec #	Parameter	Conditions	Min	Typ	Max	Units
Set Up Time						
27100	SDIO to Rising CK		10			ns
27110	STB to Rising CK		10			ns
Hold Time						
27120	SDIO to Rising CK		10			ns
27130	STB to Rising CK		10			ns
Propagation Delay						
27180	Rising CK to SDIO Out				18	ns
Pulse Width						
27140	CK Minimum Pulse Width High		18			ns
27150	CK Minimum Pulse Width Low		15			ns
27160	CK Period		40		100	ns
27170	Reset Minimum Pulse Width		100			ns



AC Characteristics - PMU

VCC = +12.5V, VEE = –3.5V, VDD = +3.3V, V_REF = 3.00V, DUT_GND = 0V unless otherwise noted. Limits established by characterization and are not production tested..

Spec #	Parameter	Conditions	Min	Typ	Max	Units
FV Settling Time						
	IR0	Measured at FORCE. Iclamps disabled; VR2; –0.8V to +6.8V. Cload = 100pF, within 0.5% of final value.		100		µs
	IR1			60		µs
	IR2			30		µs
	IR3			20		µs
	IR4			16		µs
	IR5			16		µs
	IR6			16		µs
	IR7			16		µs
FI Settling Time						
	IR0	Measured at FORCE. FI = ±Imax, Vclamps disabled. Con-FS = 1, Cload = 100pF. Rload - 2 * Rsense to ground. Measured to 0.5% of FV.		620		µs
	IR1			130		µs
	IR2			45		µs
	IR3			25		µs
	IR4			25		µs
	IR5			25		µs
	IR6			30		µs
	IR7			30		µs
	MV Settling Time	Note 1		0.5		µs
MI Settling Time						
	IR0	FV mode. ±Imax. V clamps disabled. Cload = 100pF. Measured to within 0.5% of final value.		130		µs
	IR1			55		µs
	IR2			28		µs
	IR3			20		µs
	IR4			20		µs
	IR5			20		µs
	IR6			25		µs
	IR7			25		µs

NOTES:
1. PMU in HiZ. Measured at MONITOR; IR7. Driving SENSE via FORCE (Con-FS = 1), –0.8V to 6.8V. Measured to 0.5% of FV.

Chip Overview

Pluto2 is a highly integrated System on a Chip pin electronics solution incorporating 8 independent Channels of:

- DPS/PMU/VI
- Pin Electronics
- Resistive Load

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.

CPU Control

All configuration set up and the writing to and reading back of the internal registers is controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. This chart shows how to program each internal signal.

Real Time Control

All real time control and observation is accomplished via the high speed input and output signals:

- DATA_0 - DATA_7 (Single Ended Inputs)
- EN_0 - EN_7 (Single Ended Inputs)
- COMP_A_0 - COMP_A_7 (Single Ended Outputs)
- COMP_B_0 - COMP_B_7 (Single Ended Outputs).

Analog References

All on chip analog levels are related to an off chip precision voltage reference:

- V_REF

This external reference is used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, part to part, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

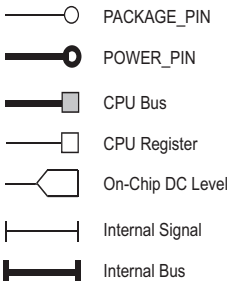
1. All capital letters (i.e. DATA_0, CK, SDIO)
2. Underscores for clarity (i.e. DATA_0, COMP_B_1)
3. Shown next to an I/O circle in any schematic.

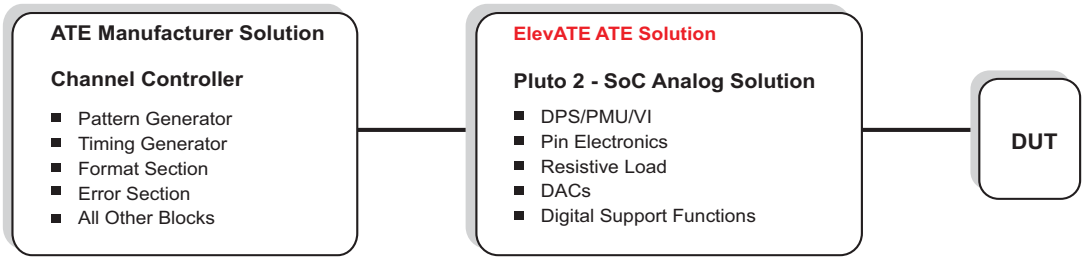
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. The first letter in a word is always a capital letter
2. Subsequent letters within the same word are small
3. Dashes (but never an underscore) for clarity
4. NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.





Changes from Pluto to Pluto2

Pluto2 is a pin and functionally compatible upgrade to Pluto. The list of changes and upgrades are listed below. New features are highlighted in yellow in the text and are highlighted in green in the schematic pictures throughout the data sheet.

Power

The power consumption per channel has been significantly reduced when the part is in the quiescent state. Independent power down options have been added to the DVL buffer and the comparator to save power when these blocks are not used.

DPS Mode

A mode has been added to support DPS applications by the CPU connecting an external compensation capacitor. The resulting performance has:

- improved dynamic response and better voltage stability vs. a change in current load
- stability under significantly larger capacitive loads.

Head Room

The head room vs. VCC and VEE has been decreased to allow a larger usable I/O range for a given set of power supplies or to support a lower set of power supplies for a given I/O range.

The values of the sense resistors have been cut in half but the MI voltage has been doubled. Therefore, the IR drop across the sense resistors is ±500 mV, but MI is +/- 1V, for ±Imax.
The on-resistance of the sense resistor select switches has been reduced.

The resistance of the EXT_FORCE switch has been reduced by roughly one half.

The resistance of the PMU connect switch has been reduced by roughly one half.

Voltage Range Shifting

A Vmid DAC has been added to allow the voltage ranges to be shifted up or down to allow a lower voltage range to be optimized for a required application I/O range without having to use a higher voltage range.

Voltage and Current Clamps

The clamp range has been expanded to allow the voltage and current clamps to function without affecting the forced or measured parameter.

Thermal Monitor

A thermal monitor has been added to allow continuous tracking of the junction temperature.

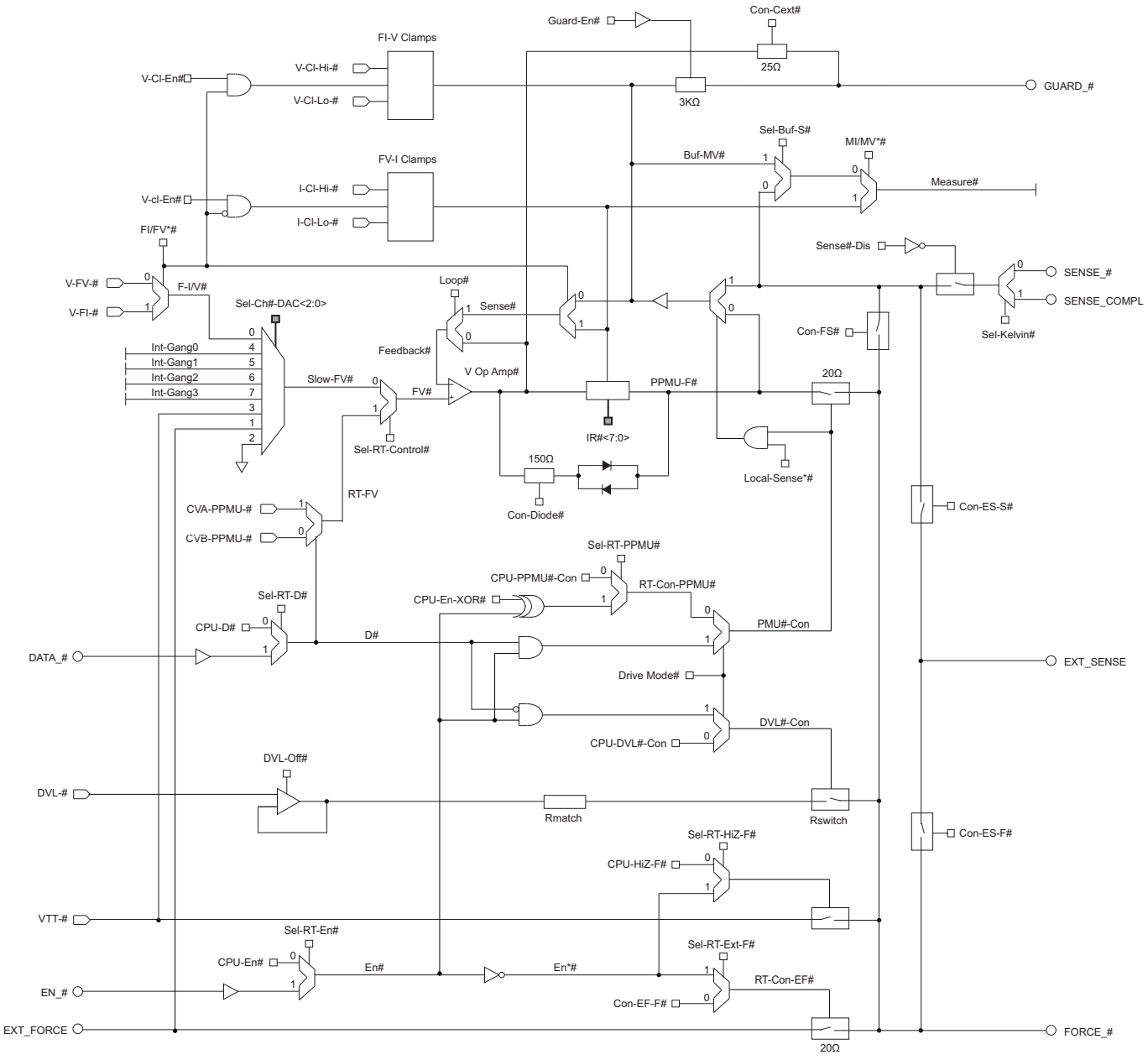
A digital output indicating an over temperature situation has been added.

Pin Electronics Mode

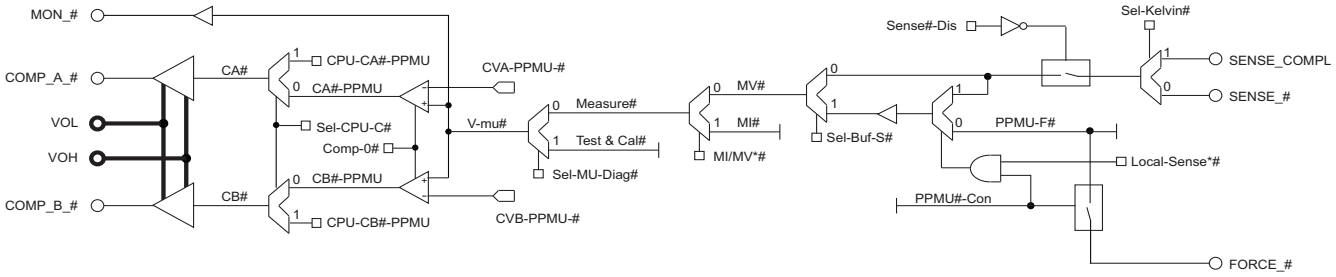
Fmax has been increased to 10MHz. The driver output impedance has been moved closer to 50Ω.

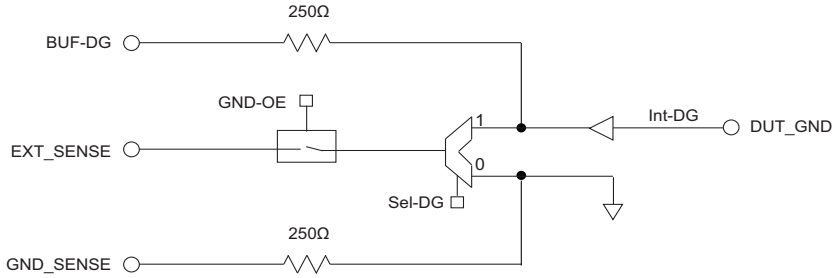
Circuit Diagrams

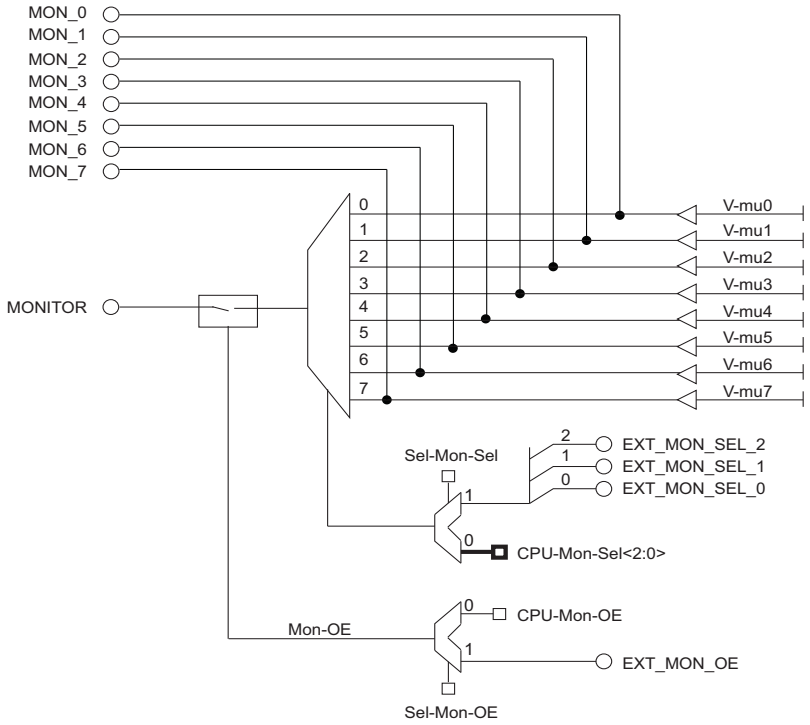
PMU Overview



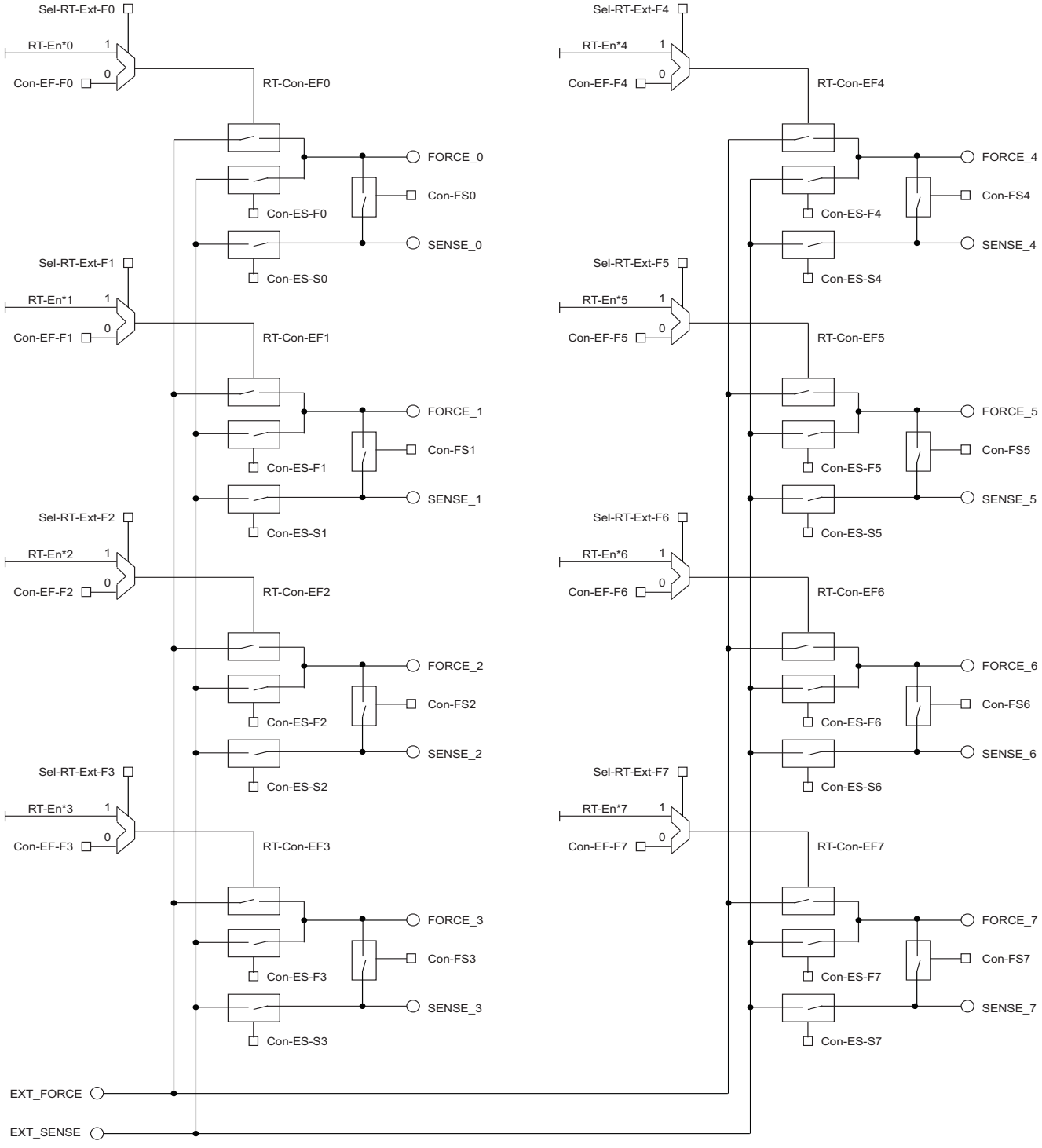
Measurement Unit



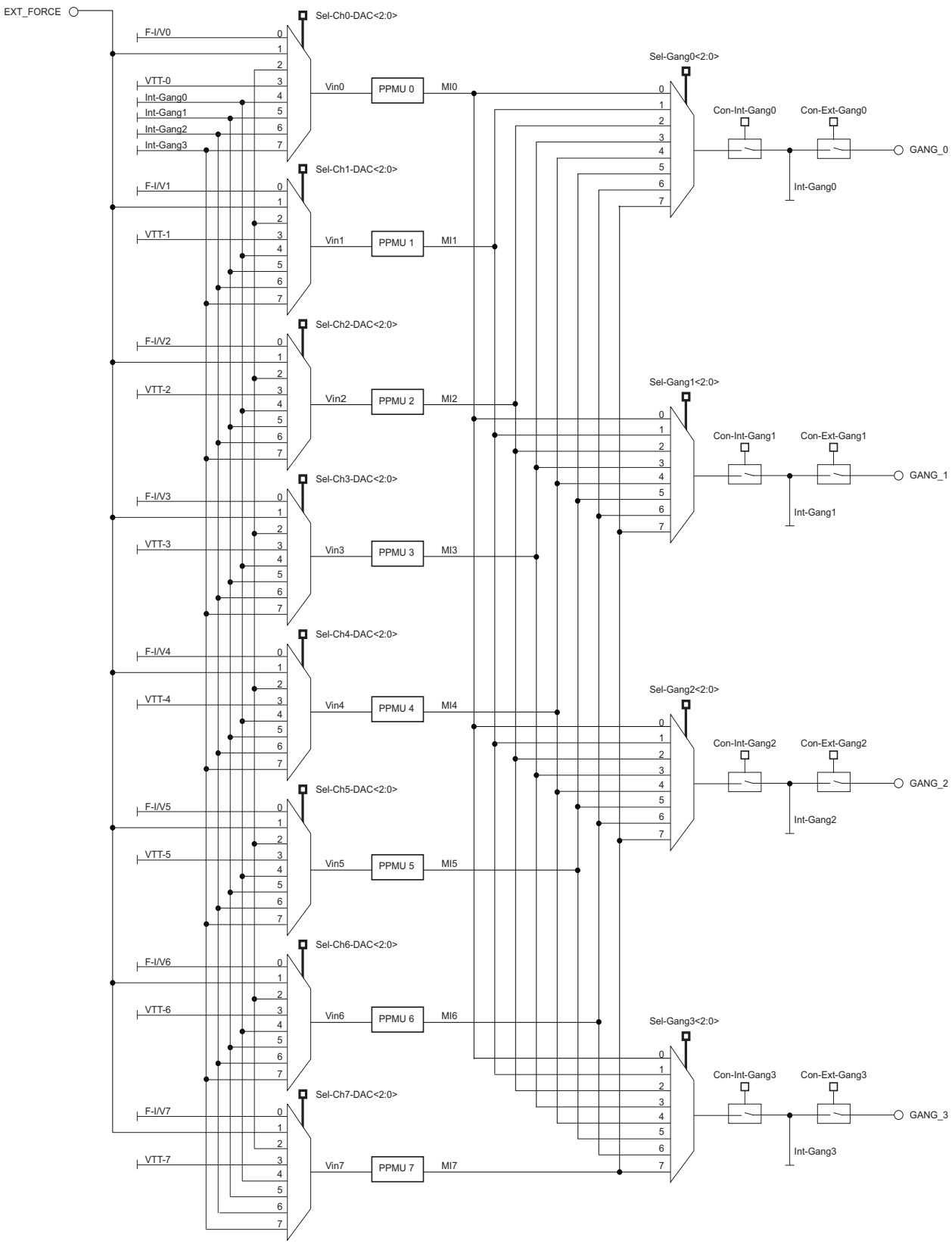




External Force/Sense Matrix



Current Ganging Matrix



PMU

Overview

Each separate Parametric Measurement Unit (PPMU) has the ability to:

- Force Voltage
- Measure Voltage
- Force Current
- Measure Current

The current or voltage measured may be tested via several paths:

- On-chip PPMU dual comparator (per channel)
- Central MONITOR (per chip)
- Per Channel MONITOR

Operating Mode

The decision whether to force current or voltage, or to measure current or voltage, is controlled by internal registers FI/FV* and MI/MV* and are programmed via the CPU port.

TABLE 8.

FI/FV*#	Ch# PPMU Force Function
0 1	Force Voltage Force Current

MI/MV*#	Ch# PPMU Meaure Function
0 1	Measure Voltage Measure Current

There are no restrictions between what is forced and what is measured. Eight combinations are possible:

- FI/MI
- FV Only
- FV/MV
- FI Only
- FV/MI
- MV Only
- FI/MV
- MI Only

Current Force

In this mode, the current being forced is set by the on-chip DC level and has the following transfer function.

TABLE 9.

V-FI#<15:0>	MI#	Current at FORCE_#
0000H 1FFFH FFFFH	–1V 0V +1V	–FImax 0 +FImax

The transfer function for FI is:

V-FI# = Iout • 2 • Rsense

The CPU port selects 1 of 8 current ranges.

TABLE 10.

IR#<7:0>	Imax	Rsense	Resolution
00000001	±2µA	250KΩ	30pA
00000010	±8µA	62.5KΩ	120pA
00000100	±32µA	15.625KΩ	477pA
00001000	±128µA	3.9KΩ	1.9nA
00010000	±512µA	976Ω	7.63nA
00100000	±2mA	244Ω	30.5nA
01000000	±8mA	61Ω	122nA
10000000	±32mA	15.26Ω	488nA

Voltage Force

The MI transfer function is:

MI# = Iout • 2 • Rsense

The CPU port selects 1 of 8 current ranges.

TABLE 11.

IR#<7:0>	MImax	Rsense	MI#
00000001	±2µA	250KΩ	±1V
00000010	±8µA	62.5KΩ	±1V
00000100	±32µA	15.625KΩ	±1V
00001000	±128µA	3.9KΩ	±1V
00010000	±512µA	976Ω	±1V
00100000	±2mA	244Ω	±1V
01000000	±8mA	61Ω	±1V
10000000	±32mA	15.26Ω	±1V
10000000	±64mA	15.26Ω	±2V

Forcing Voltage Options

There are multiple options for the input voltage to the PPMu forcing op amp. The selection is under CPU control.

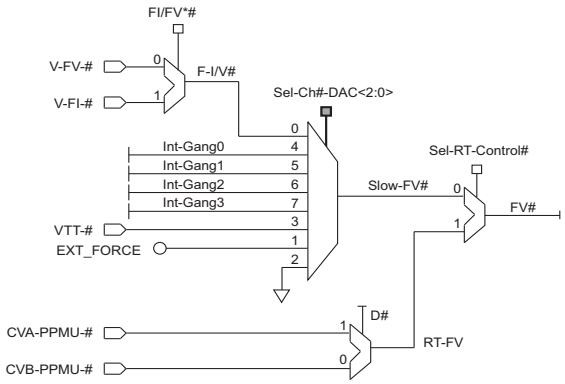


FIGURE 1.

TABLE 12.

Sel-RT-Control#	D#	Sel-Ch#-DAC<2:0>	FI/FV*#	FV#	Mode
0	X	0	0	V-FV-#	FV
0	X	0	1	V-FI-#	FI
0	X	1	X	EXT_FORCE	X
0	X	2	X	GND	FV
0	X	3	X	VTT-#	
0	X	4-7	X	Int-Gang<0:3>	FI
1	0	X	X	CVB-PPMU-#	Driver
1	1	X	X	CVA-PPMU-#	Driver

DPS Mode

The forcing op amp can change its compensation in order to:

1. be more stable under large capacitive loads
2. have a faster settling transient response when the DUT undergoes a change in load currents

TABLE 13.

Con-Ext	External Compensation Capacitor
0 1	Disconnected Connected

In order to take advantage of DPS mode, each channel requires one external capacitor placed across the FORCE and GUARD pins. the value of the external capacitor is determined by the amount of load capacitance while still being stable using the relationship:

Cext = 0.1 • Cload (max)

Recommended Cext# = 220nF.

Guard

A buffered version of the SENSE pin is brought out off-chip and may be used to drive a guard trace in any sensitive current measurement applications.

Guard Isolation

The CPU port can connect or disconnect the guard forcing voltage.

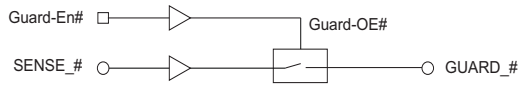


FIGURE 2.

TABLE 14.

Guard-En#	GUARD
0 1	HiZ Active

In DPS mode, the guard pin should be isolated from the buffer that normally sets the guard voltage.

Diode Bypass

Bypass diodes may be connected in parallel with the sense resistor to provide a path for transient current flow.

TABLE 15.

Con-Diode#	Bypass Diodes
0 1	Disconnected Connected

The bypass diodes are used to:

1. Allow large transient currents to flow when the PMU is in a low current range
2. Allow large capacitive loads to charge and discharge quickly when the PMU is in a low current range.

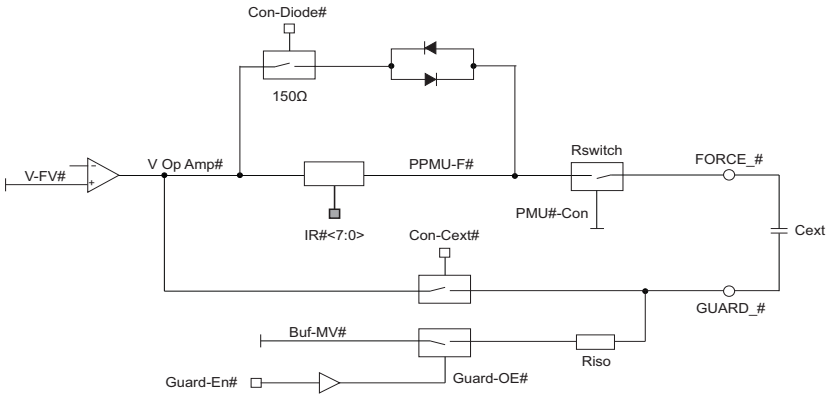


FIGURE 3.

Measurement Unit

The measurement unit generates a voltage output (V-mu#) that corresponds to the parameter being measured. There are multiple sources of parameters for V-mu:

- current at FORCE (MI)
- buffered voltage at PMU force node (MV)
- buffered voltage at SENSE (MV)
- unbuffered voltage at SENSE (MV)
- internal diagnostic node (Test & Cal)
- voltage at the complement SENSE (MV)

TABLE 16.

Sel-MU-Diag#	MI/MV*#	Sel-Buf-S#	Local-Sense*#	PMU#-Con	Sel-Kelvin#	V-mu#	Mode
1	X	X	X	X	X	Test & Cal#	Diagnostic
0	1	X	X	X	X	MI#	MI
0	0	0	X	X	0	SENSE_#	MV
0	0	1	0	X	X	PPMU_F#	MV
0	0	1	X	0	X	PPMU_F#	MV
0	0	1	1	1	0	SENSE_#	MV
0	0	X	1	1	1	SENSE_COMPL	MV

Once the V-mu source is selected, there are 2 methods to measure and test the parameter:

- Go/No Go testing
- Analog measurement

Go/No Go Testing

An on chip window comparator allows 2 bit "Go/No Go" testing. V-mu is the voltage output of the measurement unit, and it corresponds either to the voltage present at SENSE or to the current flowing through FORCE. V-mu is the input to the PPMU window comparator, whose thresholds are set with on chip DC levels through the CPU port.

The results are routed off chip through the output pins COMP_A and COMP_B and may be processed by the error section of the timing generator.

Internal State Read Back

The window comparator outputs CA#-PPMU and CB#-PPMU may be read back through the CPU port, granting direct access to the actual comparator states at any time. Otherwise, these comparator outputs may be processed as a real time test vector.

CPU Comparator Override

The CPU may override the measurement unit and set the comparator outputs COMP_A and COMP_B directly, allowing the outputs to be placed in a known state. This feature is used typically for system diagnostic purposes.

TABLE 17.

Sel-CPU-C#	COMP_A(B)_#	Configuration
0	CA(B)#-PPMU	PPMU Control
1	CPU-CA(B)#-PPMU	CPU Control

Comparator Power Down

The comparators may be powered down as a means of reducing overall power consumption in applications that do not use the functional window comparator.

TABLE 18.

Comp-Off#	Comparator mode
0	Active
1	Powered Down

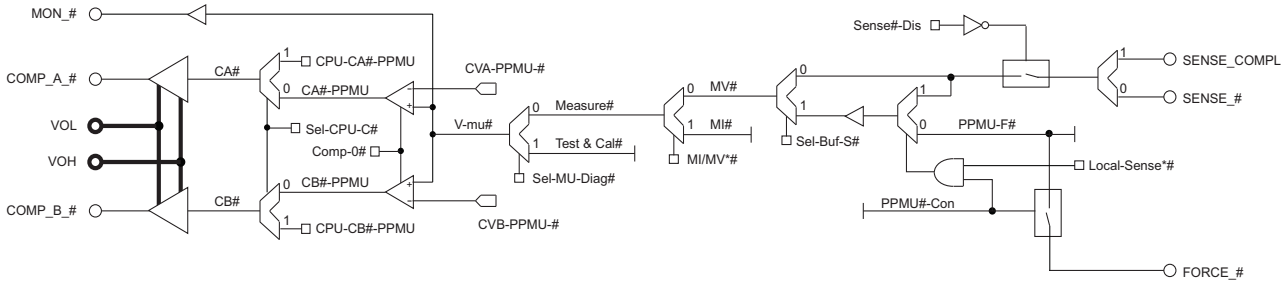


FIGURE 4.

Comparator Output Stage

Each channel supports two comparator outputs (COMP_A and COMP_B) with the following characteristics:

1. Single ended outputs
2. 50Ω series terminated outputs
3. Programmable high and low levels

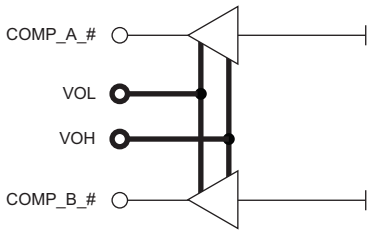


FIGURE 5.

Comparator Output Supply Levels

VOH and VOL are voltage power supply inputs that set the high and low level of COMP_A and COMP_B. VOH and VOL must also provide the current required to drive the off chip transmission line and any DC current associated with any termination used. Therefore, these inputs should be driven by a low impedance and low inductance source with ample current drive.

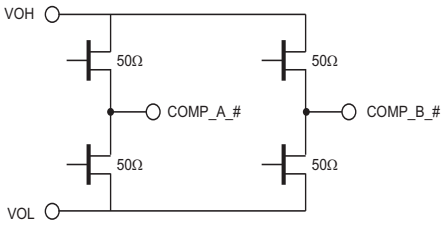


FIGURE 6.

Comparator Source Termination

In this configuration no external components are required and a full amplitude signal is realized at the destination.

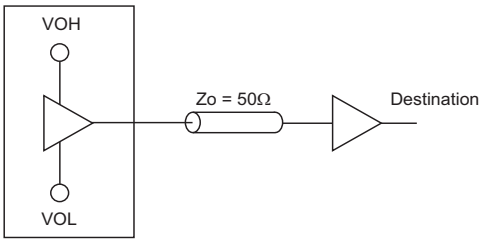


FIGURE 7.

Comparator Source and Destination Termination

In this configuration one external component is required and a 50% amplitude signal is realized at the destination.

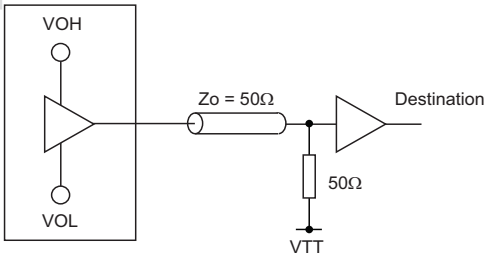


FIGURE 8.

Analog Measurement

There is a central monitor function that provides direct access to the analog voltage at the measurement unit (V-mu) of the selected channel so that an off chip Analog to Digital Converter may then calculate the value of the parameter being measured.

There are two methods for selecting the MONITOR source:

1. CPU control
2. External control

The external option allows direct real time control over which channel connects to the MONITOR and when the MONITOR is placed into a HiZ state.

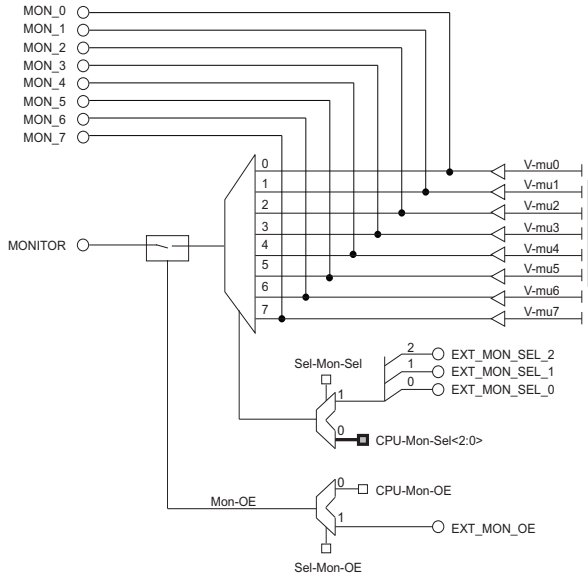


FIGURE 9.

Monitor High Impedance

MONITOR may also be place into a high impedance state.

TABLE 19.

Sel-Mon-OE	CPU-Mon-OE	EXT_MON_OE	Sel-Mon-Sel	CPU-Mon-Sel<#>	EXT_MON_SEL<#>	MONITOR
0 1	0 X	X 0	X X	X X	X X	HiZ HiZ
0 1	1 X	X 1	0 0	# #	X X	V-mu# V-mu#
0 1	1 X	X 1	1 1	X X	# #	V-mu# V-mu#

Monitor Transfer Function

When measuring voltage, MONITOR has a 1:1 transfer function with SENSE. When measuring current, MONITOR varies between -1V and +1V for -Imax and +Imax at FORCE. In the FV/MI mode the PMU is rated to provide up to ±2 • Imax for any given current range. The voltage on MI will therefore range between ±2V to support the higher currents.

TABLE 20.

Mode	Parameter	MONITOR
MV	V at SENSE_#	V (SENSE_#)
MI	–2 • MImax at FORCE_#	–2V
	–FImax at FORCE_#	–1V
	0	0
	+FImax at FORCE_#	+1V
	2 • MImax at FORCE_#	+2V

Differential Monitor

The MONITOR voltage is relative to DUT_GND when measuring voltage and relative to GND when measuring current. A differential MONITOR signal may be created by connecting MONITOR and EXT_SENSE to the two inputs of an off chip analog to digital converter.

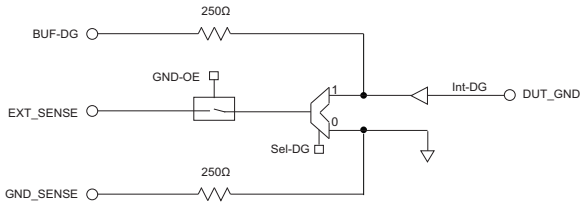


FIGURE 10.

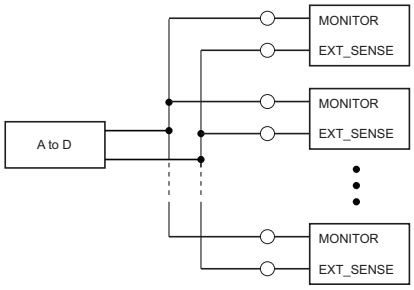


FIGURE 10.

GND-OE	Sel-DG	EXT_SENSE
0	X	HiZ
1	0	Chip Gnd
1	1	DUT_GND

NOTE: All other nodes must be disconnected from EXT_SENSE when using it as an output pin for a differential MONITOR.

Sense Options

The sense path is used to precisely control either the voltage at either the FORCE or SENSE or the current present at FORCE, and can lock on 4 different parameters:

- Current at FORCE (FI)
- Voltage at SENSE (FV)
- Op Amp output (V op amp (Tight Loop))
- Voltage at PPMU-F (Local Sense)
- Voltage at the complement SENSE (FV)

TABLE 21.

Loop#	FI/FV-#	Local-Sense*-#	PMU#-Con	Sel-Kelvin#	Feedack#	Configuration
0	X	X	X	X	V op amp#	Tight Loop
1	1	X	X	X	MI#	FI
1	0	0	X	X	PPMU-F#	FV
1	0	X	0	X	PPMU-F#	FV
1	0	1	1	0	SENSE-#	FV
1	0	1	1	1	SENSE_COMPL	FV

The local sense configuration is forced whenever Local Sense* = 0 or the switch between the PPMU-F and FORCE is open (RT-Con-PMU# = 0.)

Sense Complement

Each channel may use its own SENSE pin or the SENSE pin of the complement channel. This feature is useful when combining channels for higher current applications.

TABLE 22.

Channel#	SENSE-COMPL
0	SENSE_1
1	SENSE_2
2	SENSE_3
3	SENSE_4
4	SENSE_5
5	SENSE_6
6	SENSE_7
7	SENSE_8

Sense Disconnect

The SENSE pin may be completely isolated from the chip via the sense disconnect switch. This isolation can be useful for calibration purposes. The default condition upon power up and reset is connected.

TABLE 23.

Sense#-Dis	SENSE Pin
0	Connected
1	Disconnected

Buffered DUT Ground

BUF_DG is an analog output pin that supplies the internal DUT ground reference used to compensate internal voltages. BUF_DG is useful as a reference level for the monitor outputs when measuring voltage.

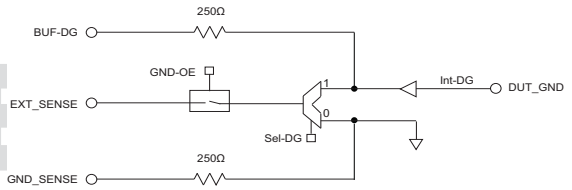


FIGURE 11.

Ground Sense

GND_SENSE is an unbuffered connection to the internal ground level. GND_SENSE should not be connected to the ground plane on the PC board. GND_SENSE should be used as a reference level for the monitor outputs when measuring current.

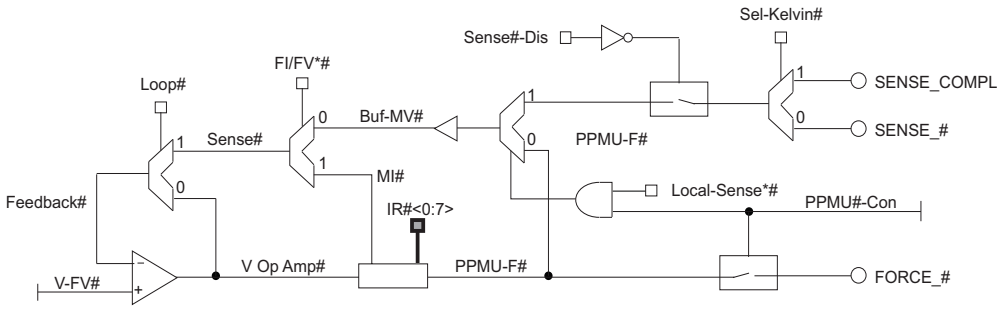


FIGURE 12.

FI Voltage Clamps

Each PPMU has programmable voltage clamps that limit the voltage swing at SENSE when the PPMU is forcing current. These clamps can be used to protect the DUT when current is being forced into a high impedance node at the DUT.

The clamps may be turned off by setting V-Cl-En = 0, in which case the clamps will remain high impedance between the supply voltages VCC and VEE.

TABLE 24.

FI/FV*#	V-Cl-En#	Ch# Clamps
0	X	Disabled
1	0	Disabled
1	1	Active

When active, the clamps sense the voltage at SENSE. If SENSE is within the limits of the high and low clamps, no action is taken. If SENSE exceeds the high or low voltage clamp, the PMU reduces the output current in order for the output voltage to not exceed the clamp. If the voltage at SENSE subsequently drops back to within the clamp levels, the PPMU resumes sourcing or sinking its programmed current.

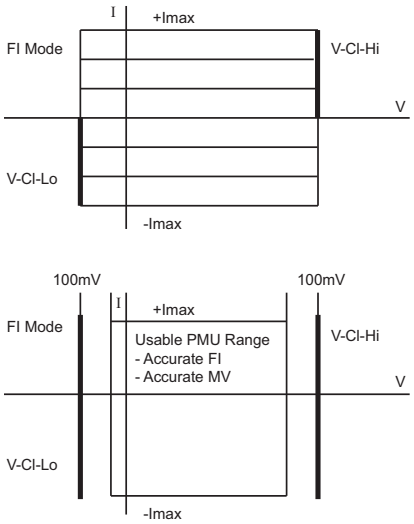


FIGURE 13.

FV Current Clamps

Each PPMU has programmable current clamps that limit the current flow at FORCE when the PPMU is forcing a voltage. These clamps are useful in protecting the DUT from an over current situation.

The clamps may be disabled by setting I-Cl-En = 0.

TABLE 25.

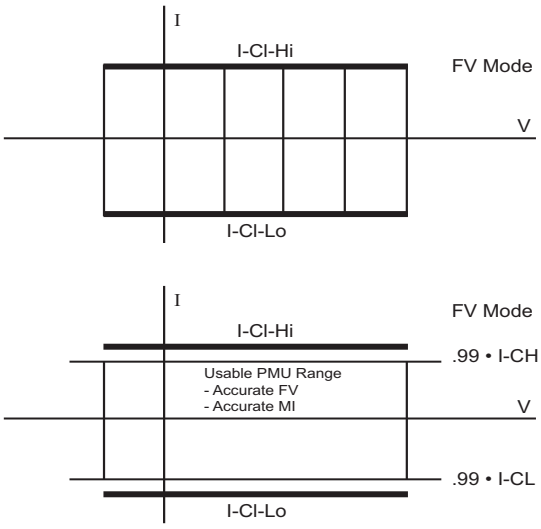
FI/FV*#	I-Cl-En#	Ch# I-Clamps
1	X	Disabled
0	0	Disabled
0	1	Active

The current clamp may be set to 3 times the value of FImax. For example, in IR7, FI max = 32mA the current clamps can be programmed as high as 96mA.

TABLE 26.

I-Cl-Hi-#<15:0> I-Cl-Lo-#<15:0>	Current Clamp Value at FORCE_#
000H	–3 • FImax
7FFFH	0
FFFFH	+3 • FImax

When Active, the I-Clamps sense the current at FORCE. If the current is within the boundaries set by I-Cl-Hi and I-Cl-Lo, no action is taken. If the measured current exceeds the upper or lower current clamp, the PMU reduces the output voltage in order for the output current to not exceed the clamps. If the current at FORCE drops back to within the clamp levels, the PPMU resumes forcing its programmed voltage.



High Current Applications

Channels may be ganged together in order to create fewer PMUs but with higher maximum currents per PMU. Up to 4 ganged PMUs per chip may be configured.

PMU Ganging

Sel-Gang#<2:0> determines which of the 8 PMUs is the master (FV Mode) and places that channel's MI# onto one of the gang nodes. When ganged together, the master PMU is placed in FV mode and all slave PMUs are placed in FI mode.

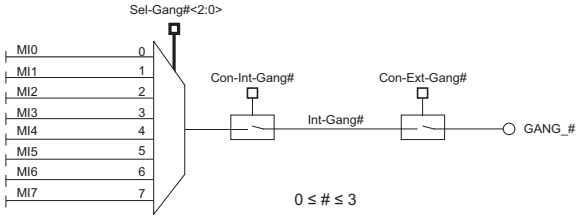


FIGURE 14.

For ganging within one IC any of the Int-Gang# nodes may be used to transmit the master MI signal as the driving voltage input to all of the slave channels. For ganging across multiple ICs, Con-Ext-Gang# must be used to route the signal all slave PMUs which reside inside a different IC.

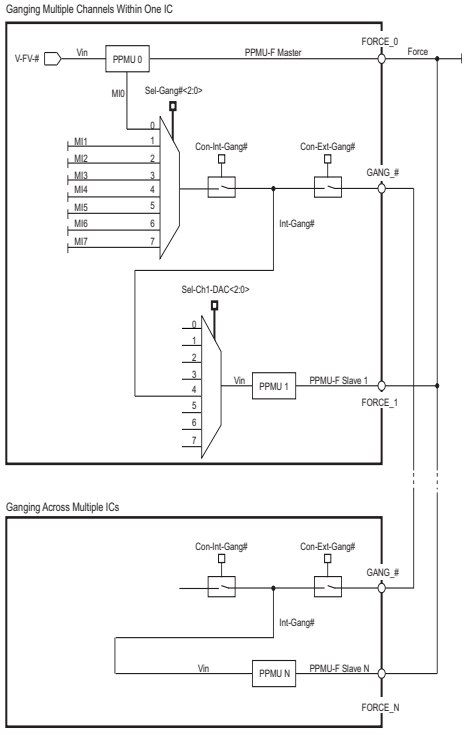


FIGURE 15.

The maximum output current is the sum of the individual output currents of the master and all slave PPMUs. To achieve this high current rating, the FORCE output pins must be connected off chip.

TABLE 27.

Con-Int-Gang#	Con-Ext-Gang#	Sel-Gang#<2:0>	Int-Gang#	# ICs
0	0	X	HiZ, No Ganging	X
1	0	0-7	Master Gang Node	1
0	1	X	Slave Gang Node	≥2
1	1	1	Master Gang Node	≥2

Remote Sense

Each channel has the ability to use its own SENSE pin or the sense or the SENSE pin of its complement channel. There are 4 sets of complementary channels per chip: 0/1, 2/3, 4/5, 6/7.

TABLE 28.

Sel-Kelvin#	Channel # Sense
0	SENSE_#
1	Complement SENSE

The complement SENSE line features is useful for implementing a Kelvin sense on a ganged high current voltage supply without having to route a FORCE and a SENSE line per channel to the DUT. In this configuration the slave PMU must be the channel complement to the master PMU.

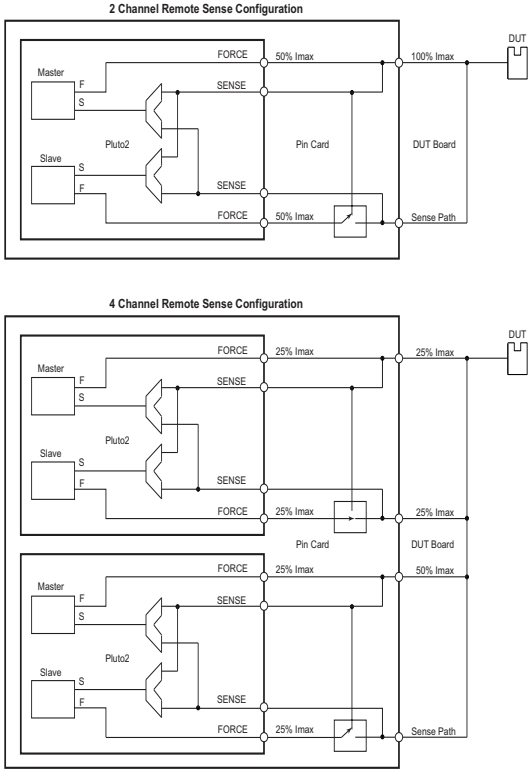


FIGURE 16.

Diagnostics

Each PPMU has access to key internal nodes so that the voltage on these nodes may be monitored. This access is typically used for testing and diagnostic purposes.

Some parameters are accessible on a per channel basis. Other nodes are central parameters that are fanned out to each channel.

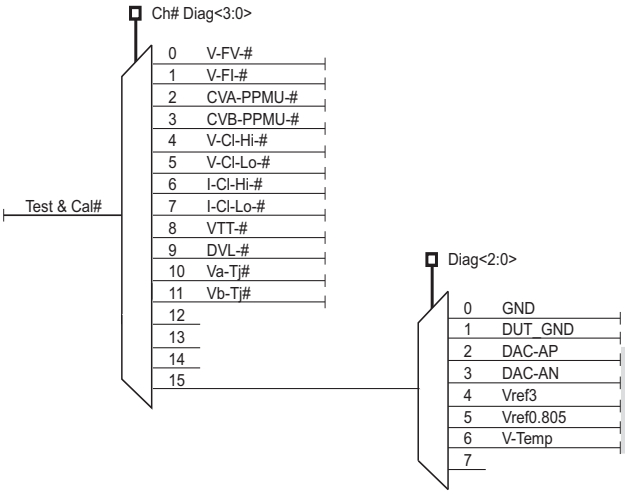


FIGURE 17.

During normal operation when the diagnostic mux is not being used the recommended settings are:

Ch# Diag<3:0> = F

Diag<2:0> = 0

This setting selects chip GND for the source voltage for all channels.

Temperature Sensing

It is possible to measure and monitor the junction temperature on a per channel basis. Test voltages Va-Tj and Vb-Tj are generated on chip and allow the calculation of the junction temperature.

The equation is:

$$Tj = \{(Va\text{-}Tj - Vb\text{-}Tj) * 1{,}637\} - 221°C$$

Va-Tj and Vb-Tj must be read back separately through the PPMU and off the chip via the MONITOR pin for the calculation to be performed.

Thermal Diode

A thermal diode allows an off-chip temperature sensor to perform continuous real time junction temperature tracking.

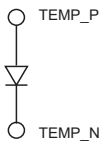


FIGURE 18.

Temperature Monitor

TJ is an analog voltage output that tracks the junction temperature. TJ may be placed in a high impedance state by the CPU port.

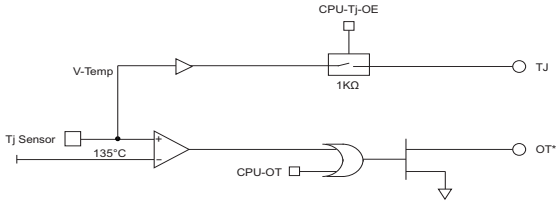


FIGURE 19.

TABLE 29.

CPU-TJ-OE	TJ
0	HiZ
1	V-Temp

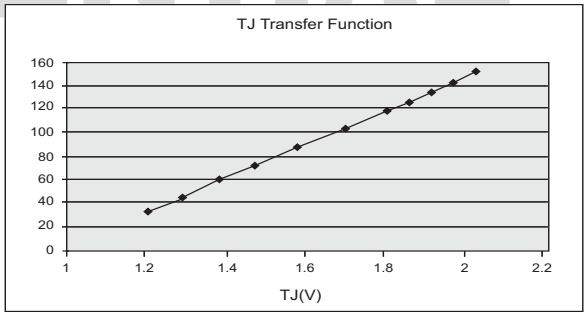


FIGURE 20.

OT* is a low voltage open drain output that indicates when the junction temperature exceeds 135°C. The CPU port can directly force the over temperature flag to be active.

TABLE 30.

CPU-OT	Junction Temperature	OT*
0	V-Temp < 135°C	HiZ
0	V-Temp > 135°C	Active, 20Ω to ground
1	X	Active, 20Ω to ground

External Force and Sense

An external force path exists to the FORCE pin of each channel. In addition, an external sense path exists to the SENSE pin and the FORCE pin of each channel. These paths are useful to bypass the PPMU completely and provide direct access to the DUT, which is useful for:

1. Connecting an external PMU to the DUT
2. Direct measurement of the DUT voltage
3. DC calibration

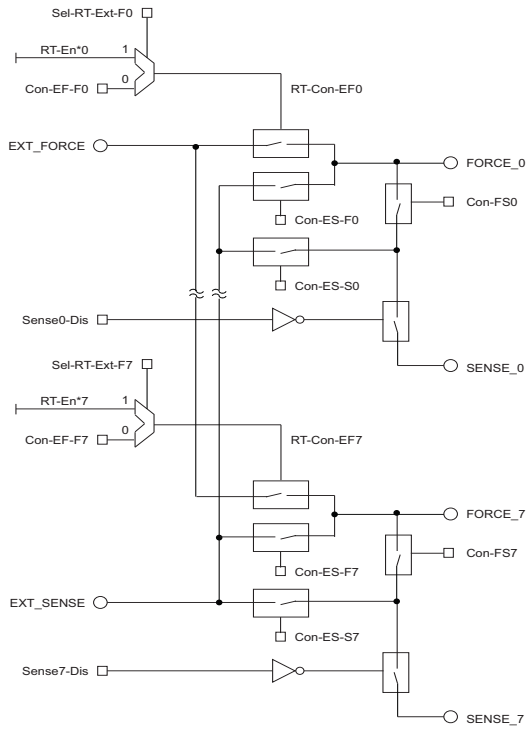


FIGURE 21.

Real Time External Force Connection

EXT_FORCE may be connected and disconnected under real time control. The CPU port can configure the EN signal to open and close the connection between EXT_FORCE and FORCE.

Each channel has independent real time connection capability to EXT_FORCE. Care must be taken to ensure that multiple FORCE pins are not erroneously connected simultaneously to EXT_FORCE..

TABLE 31.

Sel-RT-Ext-F#	RT-EN*#	Con-EF-F#	RT-Con#	FORCE_# to EXT_FORCE
0	X	0	0	Disconnected
0	X	1	1	Connected
1	0	X	0	Disconnected
1	1	X	1	Connected

TABLE 32.

Con-ES-F#	FORCE_# to EXT_SENSE
0 1	Disconnected connected

Con-ES-S#	SENSE_# to EXT_SENSE
0 1	Disconnected connected

PPMU Force/Sense Connection

Each channel may connect its Force and Sense pins internally. This direct connection allows the FV loop to be closed without connecting the FORCE and SENSE pins externally.

TABLE 33.

Con-FS#	PPMU-F to PPMU-S
0 1	Disconnected connected

Real Time PPMU Connection

There is a switch between PPMU-F and FORCE that connects and disconnects these two nodes. The high speed EN input is used to allow pattern control over when to connect and disconnect the PPMU.

An XOR gate in series with RT-En# allows either parity of EN to control the switch, as some applications (resistive load, for example) require the PPMU to be connected during a driver disable, while other applications (PPMU as a pin electronics driver) require the PPMU to be connected during a driver enable.

In addition, the CPU port can take direct control over the switch and override all real time input.

TABLE 34.

Drive Mode	Sel-RT-PPMU#	CPU-PPMU#-Con	CPU-En-XOR#	RT-En#	PMU#-Con	Channel # Real Time PPMU Switch
1	X	X	X	X		N/A
0 0	0 0	0 1	X X	X X	0 1	Disconnected Connected
0 0	1 1	X X	0 0	0 1	0 1	Disconnected Connected
0 0	1 1	X X	1 1	0 1	1 0	Connected Disconnected

Fast Drive Mode

Each PPMU is designed with the ability to behave like a traditional 2 level driver that can:

1. Force high (V-FV-#)
2. Force low (DVL-#)
3. HiZ

TABLE 35.

Drive Mode#	RT-En#	RT-D#	FORCE_#
0	X	X	X
1	0	X	HiZ
1	1	0	DVL-#
1	1	1	V-FV-#

By placing the PMU in Fast Drive Mode, each channel may independently toggle between two DC levels (V-FV and DVL) under real time DATA and EN control.

Fast Driver Mode Configuration

Sel-RT-Control# = 0

Sel-Ch#-DAC<2:0> = 0

FI / FV* = 0.

DVL Switch

If the channel is not placed in Fast Drive Mode, the CPU port has the ability to turn on and off the switches between the FORCE output pin and the on chip channel buffers.

TABLE 36.

Drive Mode#	CPU-DVL#-Con	FORCE_#
0 0	0 1	HiZ DVL

DVL Power Down

The DVL buffer may be turned off to save power consumption in applications that do not require driver.

TABLE 37.

DVL-Off#	DVL Buffer#
0 1	Active Powered Off

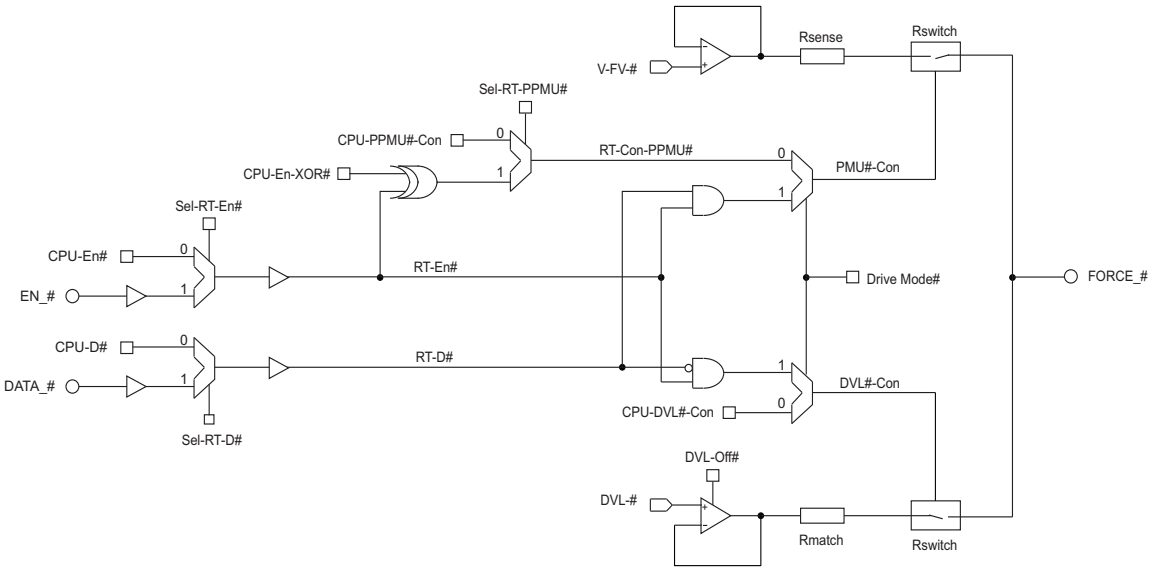


FIGURE 22.

Soft HiZ Force

Each channel supports an independent soft HiZ force function that drives the FORCE_# pin to a programmed level (VTT-#) through a 1KΩ FET switch whenever the high speed driver is placed into a high impedance state.

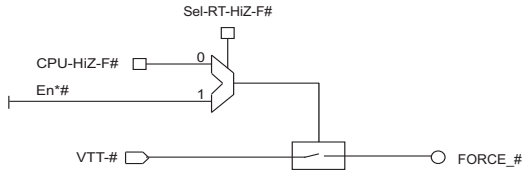


FIGURE 23.

TABLE 38.

Sel-RT-HIZ-F#	CPU-HIZ-F#	EN*#	VTT-# to FORCE_#
0	0	X	Disconnected
0	1	X	1KΩ Connection
1	X	0	1KΩ Connection
1	X	1	Disconnected

Slow Drive Mode

In addition to being able to toggle back and forth between two static levels, the PMU may be configured as a traditional driver where the PMU forcing op amp drives both the high and the low levels.

To configure the PPMU as a driver, the PPMU must be placed in FV mode and the control signals Data and Enable must exercise control over the PPMU.

TABLE 39.

Sel-RT-Control#	Sel-RT-D# Sel-RT-En#	PPMU Configuration	Control
0	X	PMU	X
1	0	Driver	CPU
1	1	Driver	Real Time

RT-D# and RT-En# determine the output state of the driver and may be under real time control or CPU control.

TABLE 40.

Sel-RT-D#	RT-D#	Sel-RT-En#	RT-En#
0	CPU-D#	0	CPU-En#
1	DATA_#	1	EN_#

The recommended configuration for the enable path is:

Sel-RT-PPMU# = 1

CPU-En-XOR# = 0

Under this set up, the PPMU behaves like a traditional driver.

TABLE 41.

RT-En#	RT-D#	FORCE_#
0	X	HiZ
1	0	CVB-PPMU-#
1	1	CVA-PPMU-#

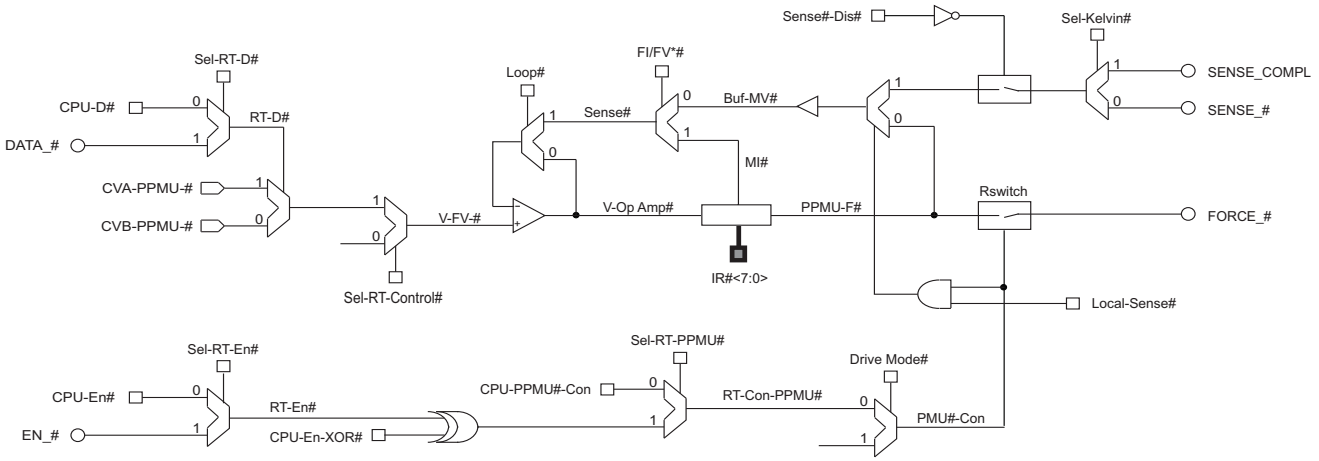


FIGURE 24.

PMU Driver Configurations

There are three ways to configure the PPMU as a driver:

1. tight loop
2. local sense
3. remote sense.

The configuration is established by the CPU port and each configuration has different driver characteristics.

Tight Loop Configuration

With Loop = 0, the PMU Op Amp will be configured as a unity gain buffer, but the PPMU itself will be open loop in that neither the voltage or the current at FORCE will be fed back into the forcing Op Amp.

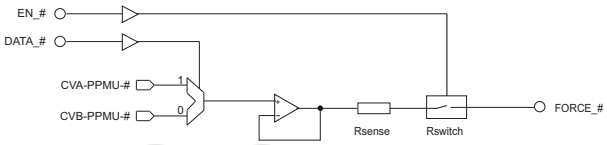


FIGURE 25.

TIGHT LOOP REGISTER CONFIGURATION

Loop# = 0

FI / FV*# = 0

Local-Sense*# = X

SELECTABLE OUTPUT RESISTANCE

In the tight loop configuration, the driver output impedance, Fmax, rise and fall times will all be determined by the value of the sense resistor, which is a function of the current range of the PPMU, and the capacitance seen at FORCE.

The total driver output impedance is the series combination of the sense resistor and the "on resistance" of the real time connection switch (Rswitch = ~50Ω.)

Rout = Rsense + Switch

The value of the sense resistor is determined by the current range selection.

TABLE 42.

Current Range	Imaz	Rsense
IR0	2μA	250KΩ
IR1	8μA	62.5KΩ
IR2	32μA	15.625KΩ
IR3	128μA	3.9KΩ
IR4	512μA	976Ω
IR5	2mA	244Ω
IR6	8mA	61Ω
IR7	32mA	15.26Ω

Local Sense Configuration

In the local sense configuration the PPMU-F voltage is fed back to the forcing op amp and a low impedance voltage source is created. The input to the op amp is toggled between CVA and CVB to create the driver pattern. HiZ is realized by opening and closing the real time switch between PPMU-F and FORCE.

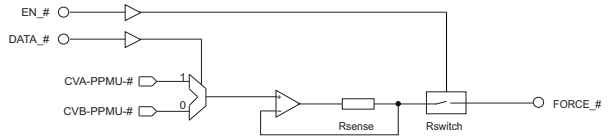


FIGURE 26.

OUTPUT RESISTANCE

The driver output impedance will be the resistance of the HiZ switch (~50Ω.)

LOCAL SENSE REGISTER CONFIGURATION

Loop# = 1

FI / FV*# = 0

Local-Sense*# = 0

Remote Sense Configuration

The PPMU in FV mode may also function as a driver by toggling between CVA and CVB at the op amp input. Since this configuration is a PMU with real time control over the forcing voltage, the resulting maximum frequency is lower than with the other configurations because of the additional resistance in the feedback path.

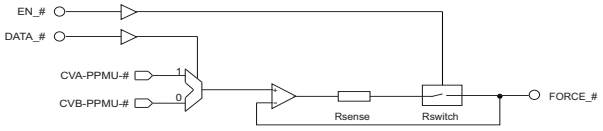


FIGURE 27.

OUTPUT RESISTANCE

The driver will have a very low DC output impedance (~0Ω).

This configuration is recommended for slower applications that require a very low output impedance or a very precise DC level at FORCE, regardless of the current flow.

REMOTE SENSE REGISTER CONFIGURATION

Loop# = 1

FI / FV*# = 0

Local-Sense*# = 1

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on chip with a 16 bit DAC that is programmed through the CPU port.

There are 4 voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group. (See Table 36 below.)

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2. If a level is programmed beyond the recommended operating conditions, saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options vs. Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

CVA-PPMU and CVB-PPMU should only use the IR range when measuring current (MI), and only use VR0, VR1, or VR2 when measuring a voltage (MV).

TABLE 43.

Range Select <1:0>	Voltage Range	Resolution (LSB)	Full Scale (FS)
0	VR0	61µV	4V
1	VR1	122µV	8V
2	VR2	244µV	16V
3	VIR	30.5µV	2V
3	VIR (I-Cl)	91.5µV	6V

Level Programming

Voltage ranges VR0, VR1 and VR2 use the equation:

Vout = (Value – Vmid) • Gain + Offset + Vmid + DUT_GND.

Current force mode (VIR) uses the equation:

Vout = (Value – Vmid) • Gain + Offset + Vmid.

Value is described by the equation:

Value = {(DAC Code) / (2**N - 1)} • FS + Vmin, where
N = 16; 2**N – 1 = 65,535

and

Vmin = Vmid – (FS/2).

Level Reference

All DC voltage levels are referenced to GND.

Vmid

The selected voltage range may be shifted up or down by the CPU port. Vmid is affects all voltage levels in all voltage ranges. Vmid does not affect current forcing and sensing DC levels. Vmid may be set independently per channel.

TABLE 44.

Vmid Value			
Vmid#<1:0>	VR0	VR1	VR2
00 01 10 11	+1.5V +1.75V +1.25V +1.0V	+3.0V +3.5V +2.5V +2.0V	+6.0V +7.0V +5.0V +4.0V
Resolution	250mV	500mV	1V

TABLE 45.

Voltage Range			
Vmid#<1:0>	VR0	VR1	VR2
00	–.5V/+3.5V	–1V/+7V	–2V/+14V
01	–.25V/+3.75V	–.5V/+7.5V	–1V/+15V
10	–.75V/+3.25V	–1.5V/+6.5V	–3V/+13V
11	–1V/+3V	–2V/+6V	–4V/+12V

Offset and Gain

Each individual DC level has independent offset and gain correction. These correction values allow the desired output level to be loaded simultaneously across multiple pins without having to correct for per pin errors.

TABLE 46.

Offset Code	Offset Value	Gain Code	Gain Value
0000H 7FFFH FFFFH	–5.4% of FS 0 +5.4% of FS	0000H 7FFFH FFFFH	0.875 1.0 1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground, and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. DUT_GND is super imposed upon all channels.

The input at DUT_GND should be:

- filtered for noise
- stable
- reflect the actual ground level at the DUT.

DUT_GND is NOT added into the DC level when forcing or measuring a current by the PPMU.

V_REF

V_REF is an analog input voltage that is used to program the on chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels.

V_REF SENSITIVITY

The above equations that predict the DAC output assume that V_REF = 3.0V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

Level = Programmed Level * (1 - (V_REF – 3.0))

Offset adjust has ample range to correct for deviations in V_REF, in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from 3.0V will not affect DC accuracy.

Required Off Chip Components

A precision reference level is required per chip.

In addition, one capacitor per channel is required to support DPS mode, but only if DPS mode is used. Cext should be selected to determine the maximum load capacitance that can be supported and still maintain stability.

Cext ≥ Cload Maximum.

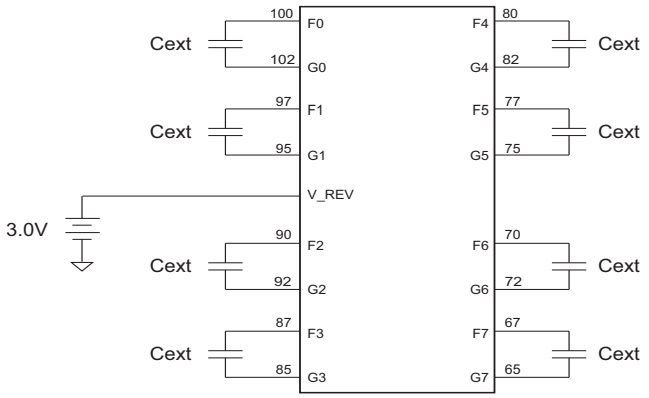


FIGURE 28.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD; VEE ≤ GND
2. VDD ≥ GND
3. VDD ≥ V_REF.

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

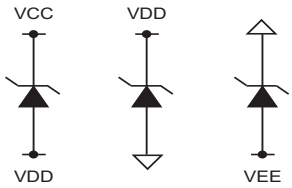


FIGURE 29.

POWER SUPPLY / ANALOG VOLTAGE SEQUENCE

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC
3. VDD
4. V_REF.

Voltage Range Options

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in the table below.

TABLE 47.

Range Decode					
Functional Block	**VR0**	**VR1**	**VR2**	**VIR**	**Range Select Bits <1:0>**
Driver **VTT, DVL**	√	√	√	√	Drive#-RS<0:1>
PPMU Comparator Thresholds **CVA-PPMU, CVB-PPMU**	√	√	√	√	PPMU#-RS<0:1>
VoltageClamps **V-Cl-HI, V-Cl-Lo** PPMU Voltage Force **V-FV**	√	√	√		FV#-RS<0:1>
PPMU Current Force **V-FI, I-Cl-HI, I-Cl-Lo**				√	N/A
Tracks DUT-GND (FV, MV)					
Does NOT Track DUT_GND (FI, MI)					

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two-point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full-scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. inner test
2. outer test.

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

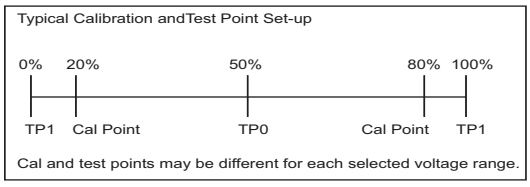


FIGURE 30.

SYSTEM LEVEL DC ACCURACY LIMITS

Other calibration schemes and techniques, using more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the offset DAC
4. Calibrate the Gain DAC
5. Calibrate the DC Level

LEVEL CALIBRATION

Initialize

- Select desired voltage range (VR0, VR1, VR2, VIR)
- Set Gain = 1.0; Offset = 0.0V

Measure

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

Calculate

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' o (Level2 - Vmid)

Finish

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

A 16-bit DAC is used to generate all of the required DC levels. To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

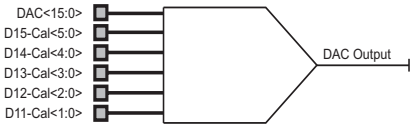


FIGURE 31.

TABLE 48. D15 Calibration

D15-Cal5	C15-Cal4	D15-Cal3	D15-Cal2	D15-Cal1	D15-Cal0	D15 Adjustment
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 49. D14 Calibration

C14-Cal4	D14-Cal3	D14-Cal2	D14-Cal1	D14-Cal0	D14 Adjustment
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	–3 LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 50. D13 Calibration

D13-Cal3	D13-Cal2	D13-Cal1	D13-Cal0	D13 Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 51. D12 Calibration

D12-Cal2	D12-Cal1	D12-Cal0	D12Adjustment
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 52. D11 Calibration

D11-Cal1	D11-Cal0	D11Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3 LSB

TABLE 53. Cal Range vs. Voltage Range vs. DAC Bits

	D15	D14	D13	D12	D11
VR0	5.67mV	2.75mV	1.28mV	549µV	183µV
VR1	11.35mV	5.5mV	2.56mV	1.1mV	366µV
VR2	22.7mV	10.1mV	5.12mV	2.2mV	732µV
VIR	2.84mV	1.38mV	640µV	275µV	91.5µV

CPU - Overview

All on chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low before another transaction may begin.

Clock Requirements

It is recommended that the CK be running at all times as it refreshes the DC levels throughout the chip. However, the CK may be stopped momentarily in order to make the chip quieter to support extremely accurate low noise measurements. The duration of these measurements should be short enough to minimize any droop on the levels.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don't care (X) value.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 54.

1st SDIO Bit	CPU Transaction Type
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Unused data bits are read back as a don't care (X) state.

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs. The parallel write is a convenient way to save time when identical information needs to go to multiple channels.

TABLE 55. Parallel Write Control

2nd SDIO Bit	CPU Transaction Type
0	Data goes to the selected channel
1	Data goes to all channels

A parallel write ignores the particular channel address, and writes the information into the same location on all channels. During a parallel write, all channels on the chip will write the data to the selected destinations in parallel, regardless of which channel's address is input into the chip.

Reset

RESET is an external hardware reset signal that places all internal registers into a low state. Reset must be executed after a power up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.**

RESET is active high.

FIGURE 32.

In addition, the CPU port can execute a reset (as a write only transaction.) If the Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 56.

Product-ID<11:0>(D15:D4)	D3 ... D0
01AH	Die Revision

Address Space

Address Description

Information is stored on-chip in two ways:

1. RAM
2. Registers

Each storage mechanism is then broken into two categories:

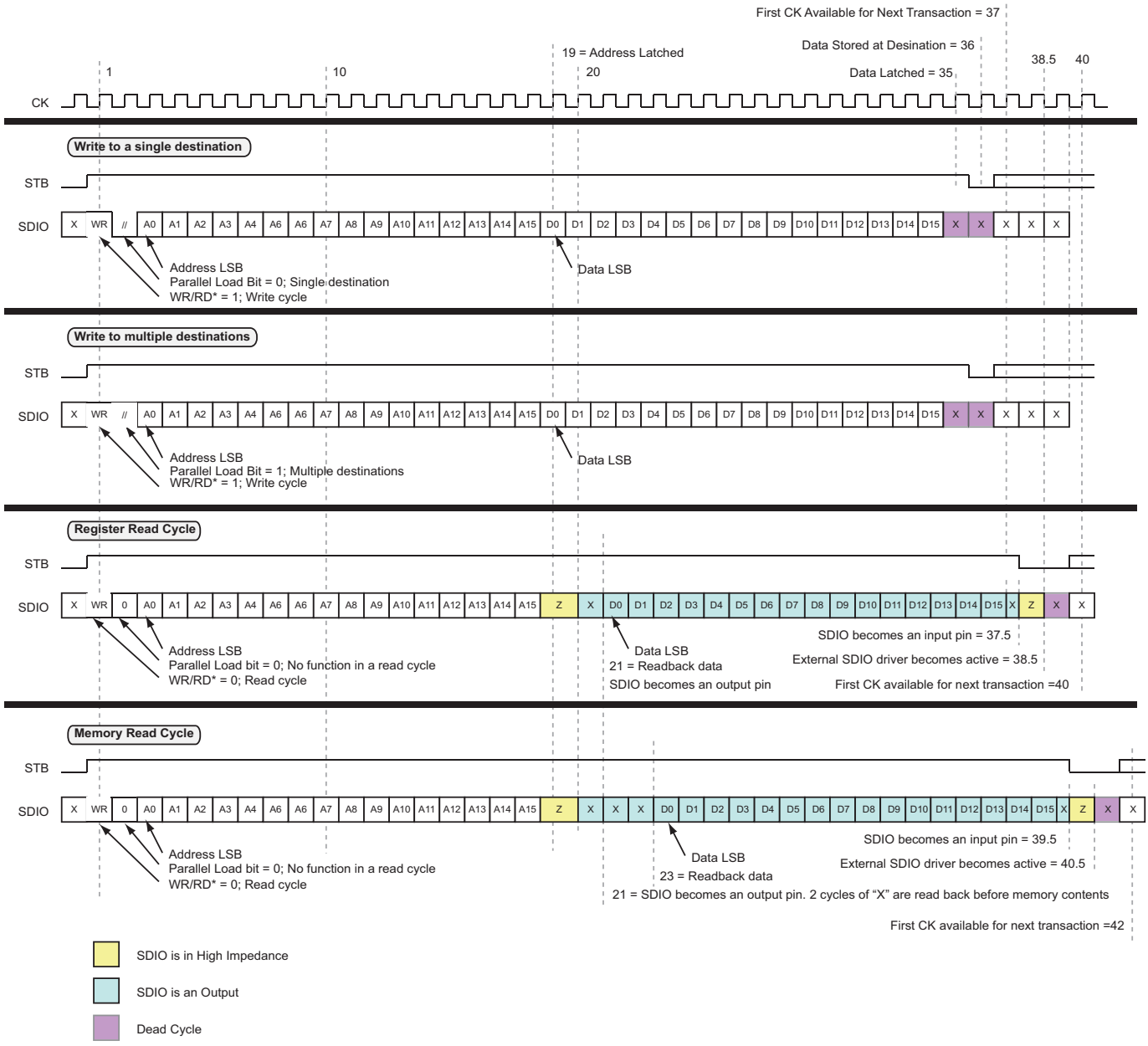
1. Per-pin resources
2. Central resources

The address space is partitioned into several different segments to clearly mark the resource type and function.

TABLE 57. Address Space

Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Channel 0 DC Levels
0	0	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Channel 0 DC Level Offset Values
0	0	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Channel 0 DC Level Gain Values
0	0	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
•	•				•				•	•			•		•	
•	•				•				•	•			•			Channels 1 – 6
•	•				•				•	•			•		•	
0	0	0	0	0	0	1	1	1	0	0	A4	A3	A2	A1	A0	Channel 7 DC Levels
0	0	0	0	0	0	1	1	1	0	1	A4	A3	A2	A1	A0	Channel 7 DC Level Offset Values
0	0	0	0	0	0	1	1	1	1	0	A4	A3	A2	A1	A0	Channel 7 DC Level Gain Values
0	0	0	0	0	0	1	1	1	1	1	A4	A3	A2	A1	A0	Not Used
Per Pin Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	0	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 0 Registers
1	0	0	0	0	0	0	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 1 Registers
1	0	0	0	0	0	0	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 2 Registers
1	0	0	0	0	0	0	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 3 Registers
1	0	0	0	0	0	1	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 4 Registers
1	0	0	0	0	0	1	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 5 Registers
1	0	0	0	0	0	1	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 6 Registers
1	0	0	0	0	0	1	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 7 Registers
Central Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Central Resource Registers

Protocol Timing Diagram



Per Pin DC Levels

Channel 0-7 RAM Storage (# = Channel Number)																
Register Bit	Central Bit	CHANNEL ADDRESS							DAC Function		RESOURCE ADDRESS					DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	0	0	VTT-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	0	1	DVL-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	1	0	CVA-PPMU-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	1	1	CVB-PPMU-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	1	0	0	V-FV-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	1	0	1	V-FI-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	1	1	0	V-CI-Hi-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	1	1	1	V-CI-Lo-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	1	0	0	0	I-CI-Hi-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	1	0	0	1	I-CI-Lo-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	10 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	0	0	VTT-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	0	1	DVL-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	1	0	CVA-PPMU-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	1	1	CVB-PPMU-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	0	1	0	0	V-FV-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	0	1	0	1	V-FI-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	0	1	1	0	V-CI-Hi-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	0	1	1	1	V-CI-Lo-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	1	0	0	0	I-CI-Hi-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7				1	0	1	0	0	1	I-CI-Lo-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	10 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	0	0	VTT-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	0	1	DVL-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	1	0	CVA-PPMU-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	1	1	CVB-PPMU-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	1	0	0	V-FV-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	1	0	1	V-FI-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	1	1	0	V-CI-Hi-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	1	1	1	V-CI-Lo-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	1	0	0	0	I-CI-Hi-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	1	0	0	1	I-CI-Lo-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	10 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			1	1	0 – 31					Not used

NOTE: Do not write to or read from any of the unused locations.

Per Pin Registers

Channel 0 – 7 Control Registers (0 ≤ # ≤ 7)																				
Register Big	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	0		WE	CPU-DVL#-Con	Drive Mode#	WE	Sel-RT-PPMU#	CPU-PPMU#-Con	CPU-En-XOR#	WE	Sel-RT-En#	CPU-En#	WE	Sel-RT-D#	CPU-D#	WE	Sel-RT-Control#	Driver Configuration
1	0	#	1								WE	IR#7	IR#6	IR#5	IR#4	IR#3	IR#2	IR#1	IR#0	Current Range
1	0	#	2	WE	I-CI-En#	WE	Sense#-Dis	WE	V-CI-En#	WE	Sel-Buf-S#	WE	Local-Sense*#	WE	Loop#	WE	MI/MV*#	WE	FI/FV*#	PPMU Configuration
1	0	#	3		CB#-PPMU	CA#-PPMU	WE	Con-FS#	WE	Sel-CPU-C#	CPU-CB#-PPMU	CPU-CA#-PPMU	WE	Sel-MU-Diag#	WE	Ch# Diag3	CH# Diag2	CH# Diag1	CH# Diag0	Diagnostics
1	0	#	4					WE	Sel-RT-HiZ-F#	CPU-HiZ-F#	WE	Drive#-RS 1	Drive#-RS 0	WE	FV#-RS 1	FV#-RS 0	WE	PPMU#-RS 1	PPMU#-RS 0	Voltage Range Selection
1	0	#	5				WE	Sel-Kelvin#	WE	Sel-Ch#-DAC 2	Sel-CH#-DAC 1	Sel-Ch#-DAC 0	WE	Con-ES-S#	WE	Con-ES-F#	WE	Sel-RT-Ext-F#	Con-EF-F#	External Force/Sense DPS Compensation
1	0	#	6							WE	Vmid#<1>	Vmid#<0>	WE	Guard-En#	Con-Diode#	Con-Cext#	WE	Comp-Off#	DVL-Off#	Power Down Options PMU Mode
1	0	#	6-127																	Not Used

Read Only

Central Resource Register

Register Big	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	0	0	WE	CPU-OT	CPU-Tj-OE	WE	Sel-Mon-Sel	WE	Sel-Mon-OE	WE	Sel-DG	GND-OE	WE	CPU-Mon-OE	WE	CPU-Mon-Sel2	CPU-Mon-Sel1	CPU-Mon-Sel0	Monitor
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reset
1	1	0	2													WE	Diag 2	Diag 1	Diag 0	Diagnostics
1	1	0	3	WE	Con-Ext-Gang1	WE	Con-Int-Gang1	WE	Sel-Gang1 2	Sel-Gang1 1	Sel-Gang1 0	WE	Con-Ext-Gang0	WE	Con-Int-Gang0	WE	Sel-Gang0 2	Sel-Gang0 1	Sel-Gang0 0	Current Ganging Nodes 0 & 1
1	1	0	4	WE	Con-Ext-Gang3	WE	Con-Int-Gang3	WE	Sel-Gang3 2	Sel-Gang3 1	Sel-Gang3 0	WE	Con-Ext-Gang2	WE	Con-Int-Gang2	WE	Sel-Gang2 2	Sel-Gang2 1	Sel-Gang2 0	Current Ganging Nodes 2 & 3
1	1	0	5				WE	D14-Cal4	D14-Cal3	D14-Cal2	D14-Cal1	D14-Cal0	WE	D15-Cal5	D15-Cal4	D15-Cal3	D15-Cal2	D15-Cal1	D15-Cal0	Upper DAC Bit Calibration
1	1	0	6					WE	D11-Cal1	D11-Cal0	WE	D12-Cal2	D12-Cal1	D12-Cal0	WE	D13-Cal3	D13-Cal2	D13-Cal1	D13 -Cal0	Mid DAC Bit Calibration
1	1	0	7 – 126																	Not Used
1	1	0	127	Product-ID11	Product-ID10	Product-ID9	Product-ID8	Product-ID7	Product-ID6	Product-ID5	Product-ID4	Product-ID3	Product-ID2	Product-ID1	Product-ID0	Die-Rev3	Die-Rev2	Die-Rev1	Die-Rev0	Die ID

Write Only

Read Only

Manufacturing Information

Moisture Sensitivity

Pluto2 is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

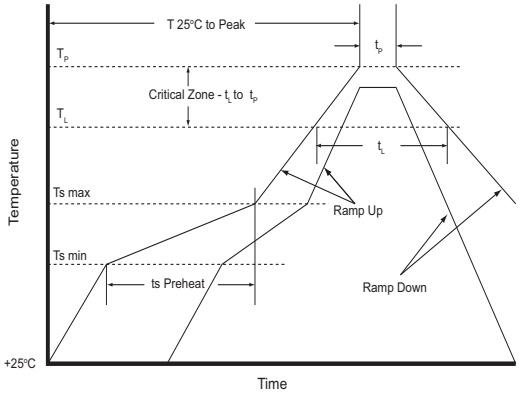
Chip Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead free or not.

PROFILE FEATURE	Pb-Free ASSEMBLY
Average ramp up rate (Ts max) to T_P)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 to 120 sec
ts max to T_p • Ramp Up Rate	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 217°C 60 to 150 sec
Peak Package Body Temperature	260°C
Time within 5°C of actual peak temp (tp)	20 to 30 sec
Average ramp down rate (Tp to Ts max)	6°C/sec (max)
Time +25°C to peak temperature	8 minutes (max)



Thermal Analysis

JUNCTION TEMPERATURE

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$$Tj = Pd \bullet \theta JA + Ta$$

Tj = Junction Temperature

Pd = Power Dissipation

θJA = Thermal Resistance (Junction to Ambient)

Ta = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

CONDUCTION

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θJC) plus the resistance from the case to ambient (θCA)

CONVECTION

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

THERMAL RESISTANCE

Each system will have its own unique cooling strategy and overall θJA. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta JA = \theta JC + \theta A$$

θCA is determined by the system environment of the part and is therefore application specific. θJC is determined by the construction of the part.

θJC Calculation

θJC = θ(silicon)

+ θ(die attach)

+ θ(paddle).

θJC = .07°C/W + .3°C/W + .006°C/W

θJC = .38°C/W.

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistivity) • Thickness / Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

INTRINSIC THERMAL CONDUCTIVITY

Die Attach Thermal Conductivity = 1.4W/M°K

Silicon Thermal Conductivity = 141.2W/M°K

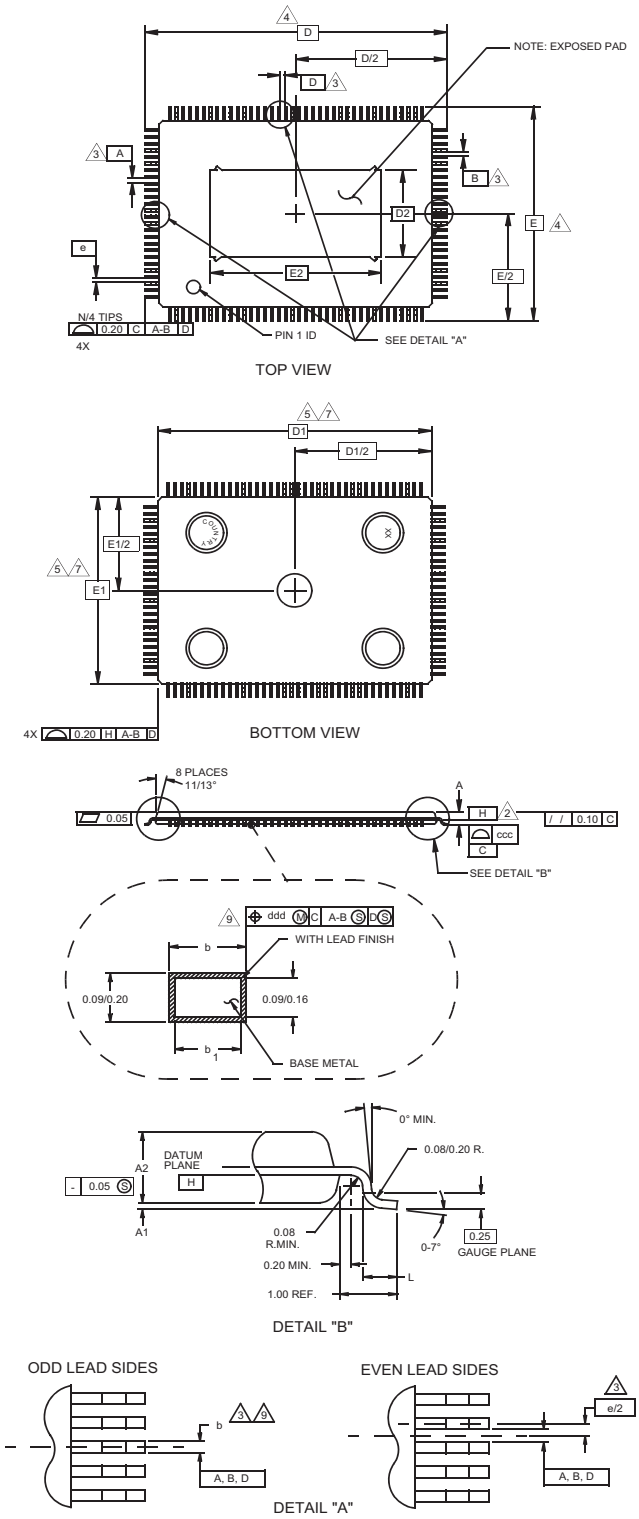
Paddle Thermal Conductivity = 263W/M°K

Plastic Thermal Conductivity = 0.88W/M°K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θJC through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic.)

Package Outline Drawing

Low Plastic Quad Flatpack Package with Top Exposed Pad (LQFP-TEP)



Q128.14x20A

128 Lead Low Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	MILLIMETERS BHB NOM	MILLIMETERS BHB MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D		22 BSC		4
D1		20 BSC		7, 8
D2		12.50 BSC		14
E		16 BSC		4
E1		14 BSC		7, 8
E2		6.5 BSC		14
L	0.45	0.60	0.75	
N		128		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

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NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

Revision History

Revision Date	Description of Changes
June 8, 2016	• Page 1: Features - 8 Current Ranges revised
January 8, 2016	• Page 49: Power Supply Sequence Section - update power supply sequence
April 1, 2015	• Reformat from Intersil to Elevate Semiconductor format

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
Pluto2-301N	Pluto2-301N	+25 to +100	128 Lead, 14x20mm TQFP w/top exposed heat slug
Pluto2-301N-LB	Evaluation Board		
Pluto2-301N–SYS	Evaluation System		

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.