ISL55161/2/3/4 and Venus Family Getting Started

Rev G01: 2012-06-11

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1 Introduction

Congratulations on your purchase of the Elevate Semiconductor ISL55161/2/3/4 and Venus Family evaluation system. You will find that it serves as an invaluable development platform to help get your product to market in the shortest possible time. The ISL55161, ISL55162, ISL55163, ISL55164, Venus, Venus3, and Venus4 products will be referred to as Venus in this document unless otherwise stated below. The Venus EVM and Graphical User Interface (GUI) allow the customer to demonstrate and evaluate the Venus performance and functionality.

This document provides the instructions to install, setup, and operate the Venus EVM. Refer to the ***Elevate Semiconductor EVM User's Guide*** for a detailed description of the EVM system.

1.1 Unpacking - Venus EVM Contents

Please check the contents of the Venus EVM shipping carton to make sure you have received all of the items listed in Table 1. The system is already configured for the best setup, except for connections to the power supply, PC controller, and test equipment.

Table 1: Venus EVM Contents

Qty	Description
1 ea.	Venus EVM System (3 boards)
1 ea.	Venus EVM Getting Started (this document)
1 ea.	Venus EVM User Interface Program Installation CD
1 ea.	DB25M-DB25M, 6 Foot Parallel Port Cable

1.2 Recommended Test and Measurement Setup

Oscilloscope, Differential Pulse Generators, DMMs, and Source Measure Unit

1.2.1 Power Supply

Table 2 provides the required power supplies and current rating. The power supplies are connected using standard banana plugs. The customer needs to provide the power supply cables.

Table 2: Power Supply Requirements

Supply	Current Rating
+20V	1 A
+5V	1 A
-15V	1 A

1.2.2 PC Controller

To use the Venus EVM User Interface Program (UIP), a PC with the following configuration is required:

- Win98, Win2000, WinNT 4.0+, or Win XP
- Parallel/Printer Port – 25-pin female connector

1.3 Software Installation

There are 2 steps to install the Venus EVM demonstration program. The first step is to install the Venus EVM UIP from the CD-ROM. The second step requires installing the parallel port driver (ParPort2k).

Figure 1 illustrates the default directory structure. The user may change the <root dir> during the installation.

Figure 1: Installation Directory Structure

<Root Dir>\Planet ATE\EVM GUI
Documents
ParPort2k

1.3.1 Venus EVM UIP Installation

To install the Venus EVM software package, simply run the SETUP program on the distribution disk and follow the prompts. The **Elevate SemiconductorATE.exe** executable will be installed in the ***Evm GUI*** sub-directory. In addition, a short-cut will be installed onto the desktop and in the **Start->Programs** folder. The **Start->Programs** folder also contains links to the different product datasheets, EVM User's Guide, and documentation folder.

1.3.2 Parallel Port (ParPort2K) Installation

To install the ParPort2K parallel port driver, run the **setup.exe** from the ***ParPort2k*** sub-directory after the main installation is complete and click the **Install** button. For WinNT users, the user must have administration rights.

Note: ParPort2k is a copyright of Zeecube Software.

1.3.3 Reboot Machine

After the Venus EVM and Parallel Port software is installed, it is recommended to re-boot the machine.

1.3.4 Launching the Venus EVM Program

The user can launch the Venus EVM GUI from the desktop, **Start->Programs** folder, or ***EVM GUI*** sub-directory.

1.3.5 Software Un-Installation

The Venus EVM demonstration program may be un-installed using the **Add/Remove Program** from the Windows Control Panel.

2 Getting Started

The Venus EVM is shipped in a pre-configured state that allows a customer to evaluate the basic driver and comparator output performance as well as the PMU Force Voltage (FV) / Force Current (FI) modes. Figure 2 provides an illustration of the recommended interconnections to the Venus EVM. However due to equipment availability, the EVM can easily and quickly be configured for different options.

2.1 Loadboard and Motherboard Revisions

There are several different loadboard revisions: Rev B, Rev C, Rev D, and Rev F+. In addition, there are several different Motherboard revisions: Rev A, Rev B, Rev C, and Rev D+.

This document only supports the Loadboard Rev F+ and the Motherboard Rev D+.

For earlier Loadboard & Motherboard revisions, please contact Elevate Semiconductor for the appropriate documentation.

2.2 Venus and ISL Product Families

The Loadboard supports all of the various Venus and ISL Products: Venus (Classic), Venus3, Venus4, ISL55161, ISL55162, ISL55163, and ISL55164. The Venus4 and ISL55163 devices redefined a handful of pins. To support the different products, the loadboard installs/removes a handful of components to support the different features. Refer to Section 3 for details. Also refer to the schematic and datasheets.

2.3 Default Configuration Setup Options

The EVM has several default options for providing a DATA stream and/or configuring for PMU mode. Each of the default configurations below may not be available for every product.

Mode	Brief Description	Reference
Hardware Reset	All registers default to the hardware default state.	None
Three-State (High-Z)	Puts Venus Driver and PMU in three-state (high-Z).	None
Real Time Data (default)	Use motherboard DATA# SMA connectors	Section 2.3.1
Ring Oscillator Mode	Use Venus's internal Ring Oscillator	Section 2.3.2
LVDS Output Levels	Use Channel #0 and #1 create a low-voltage differential signal	Section 2.3.3
Chan#0 RT DATA Chan#1 Compare Only	Configures Venus so can evaluate Drive/Compare on Channel #0 and Compare Only on Channel #1	Section 2.3.4
PMU FV or FI	Configures both channels to the desired mode	Section 2.3.5
PMU Chan #0 FV and Chan #1 FI	Use the other channel to provide current/voltage load	Section 2.3.6
Real Time SV / DVL	Use Real Time EN input to toggle between SV (FV) and DVL. Optionally can use SV input to toggle between SV and HiZ.	Section 2.3.7

2.3.1 Real Time Data

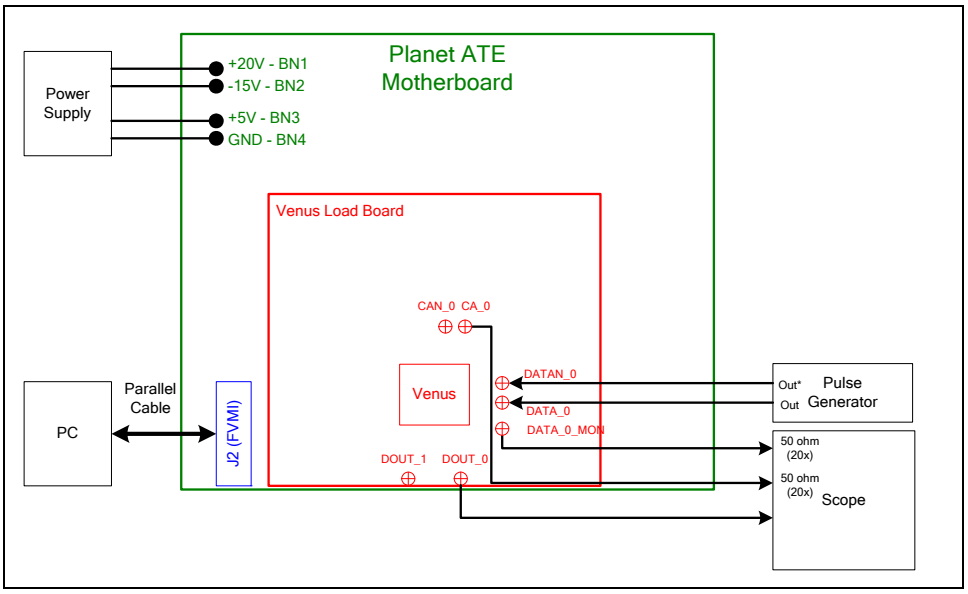
Figure 2 illustrates the recommended EVM configuration. This option sources the DATA# from a Pulse Generator. The ENABLE# is set to CPU Control and high (always enabled). The SV# is set to CPU Control and low (always disabled/open). The DATA# input term is set to 100 Ohm. This option works best if the customer has a differential pulse generator with at least a 200mV swing.

The DATA#_MON and Comparator Outputs (CA#) have a 953 ohm pick-off. The scope should be set to 50 ohm termination with an attenuation factor of 20.

Note: Channel #1 could be connected in a similar fashion, not shown in diagram. Both channels are configured the same.

If the customer only has a single ended pulse generator, then the DATAN# can be tied to 1.0V (Vterm); the Vterm must be able to handle any current flow required for proper termination. Set the pulse generator to a 0.0V to 3.0V swing. Select the **Single Ended RT Data** from the **EVM Setup** configuration menu. The DATA# input term is set to NONE.

Figure 2: Real Time DATA Block Diagram

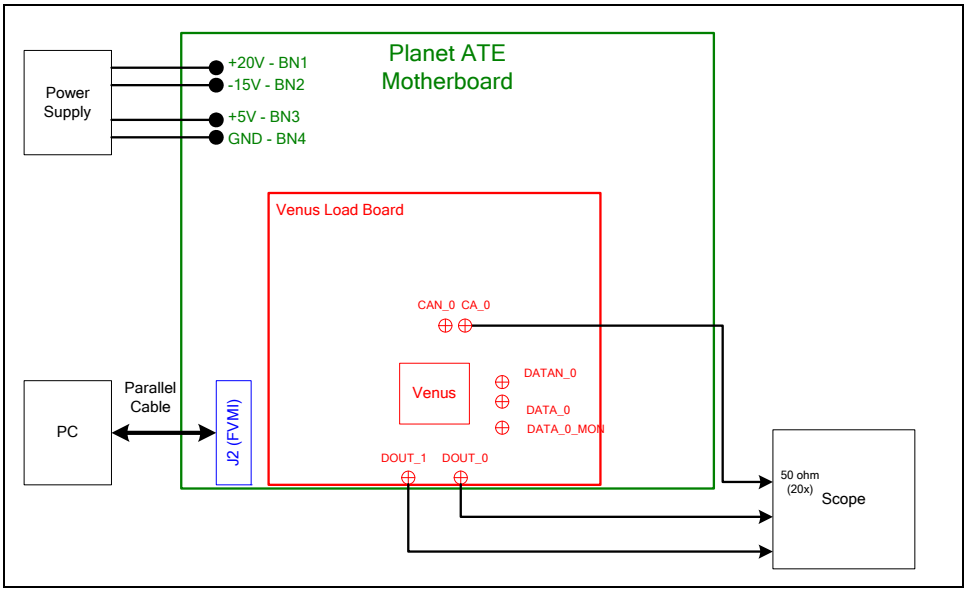


2.3.2 Ring Oscillator Mode (No Pulse Generator)

Figure 3 illustrates a possible configuration for customers without any pulse generator. This option uses the Venus Ring Oscillator feature to generate a ~20 MHz pulse with a ~15 nS pulse width. All deskews are enabled and set to zero delay. Both channels are configured the same.

The Comparator Outputs (CA#) have a 953 ohm pick-off. The scope should be set to 50 ohm termination with an attenuation factor of 20.

Figure 3: Ring Oscillator Block Diagram



2.3.3 LVDS Outputs Real Time Data

Figure 2 illustrates the EVM configuration for generating LVDS Outputs. A Low Voltage Differential Signal (LVDS) is defined as Vcm=1.25V and Vswing=350mV into a 100 Ohm termination.

The input data stream is feed into DATA#0. Channel #1 also sources its data from DATA #0 using Venus's internal cross point switch. The Channel #1 signal is then inverted using the DATA-XOR feature. The driver DVH/DVL levels are programmed to 1.6V and 0.9V respectively. The ENABLE# is set to CPU Control and high (always enabled). The SV# is set to CPU Control and low (always disabled/open). The DATA# input term is set to 100 Ohm.

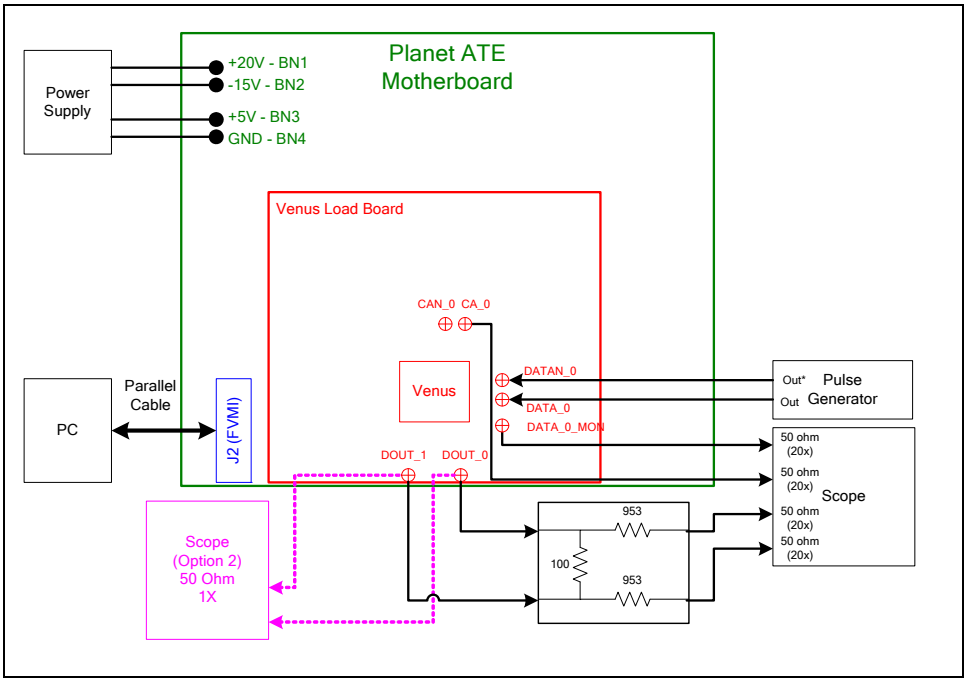
The user is responsible for programming the deskew values such that the 2 waveforms align. Failure to program the deskew values could result in poor output waveforms. The Driver Deskew Delay and Falling Edge Adjust (FEA) are enabled and set to 0.

There are 2 options to connecting the outputs to a scope.

Scope setup option 1: (true LVDS levels)
Connect a 100 Ohm resistor between DOUT0 and DOUT1. Use a 953 Ohm pick off connected to the Scope's 50 Ohm input. This will result in a 20X attenuation, the scope should be configured accordingly. The 953 Ohm pick off is used to minimize reflections, this will also cause a 5% drop in the output voltages.

Scope setup option 2: (pseudo LVDS levels)
Connect the DOUT0 and DOUT1 to the Scope's 50 Ohm input, the probe attenuation should be set to 1. The scope's two 50 Ohm resistors are used to create a 100 Ohm termination between Channel #0 and Channel #1. The main difference is that the Vcm will be 0V (GND) instead of 1.25V. The user needs to program the driver DVH/DVL to +0.350V and -0.350V respectively.

Figure 4: LVDS Output Real Time DATA Block Diagram



2.3.4 Channel #0 in Real Time DATA and Channel #1 in Compare Only

Figure 5 illustrates a possible configuration for customers to evaluate the Driver and Compare only modes. To evaluate the Driver, connect a differential pulse generator to the DATA_0 SMAs. To evaluate the Comparator Only mode, connect a single-ended pulse generator into the Venus DOUT_1 SMA.

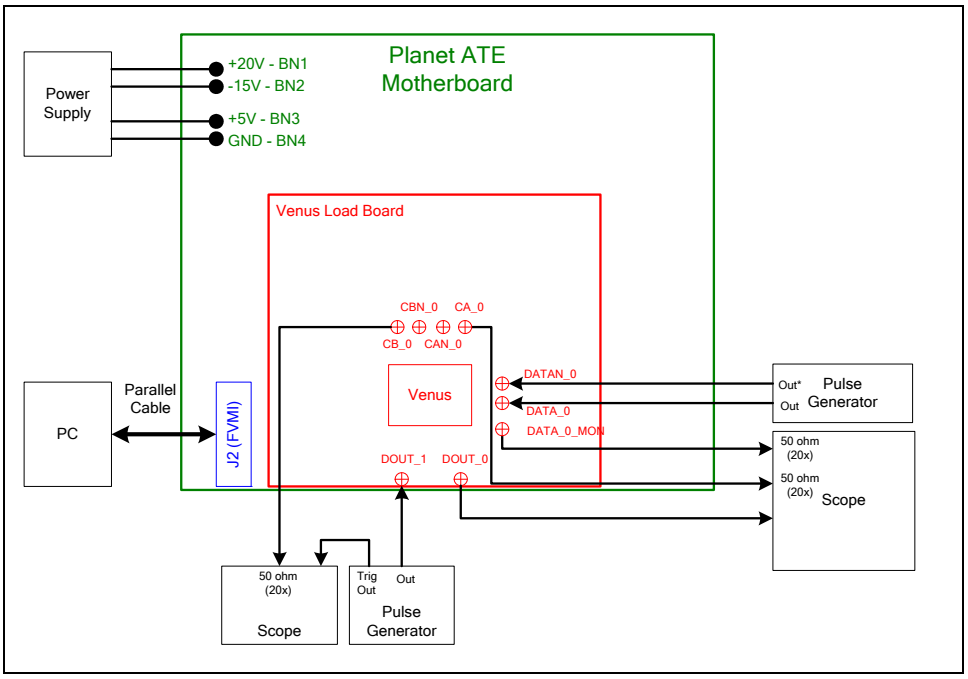
Channel#1 will be set to VTT Mode (50 Ohm termination) with the VTT Level set to 1.5V. The Channel#1 comparator thresholds are also set to 1.5V. The pulse generator should be set to swing around 1.5V. If other pulse generator levels are required, change the Venus VTT level and comparator thresholds as required.

Note: to put Channel#1 into HiZ mode instead of VTT mode, change the **DR-Mode** setting found in ***Venus->Channel 1->Driver Path Config***

The 2 channels will run asynchronously since the 2 pulse generators are asynchronous.

The DATA#_MON and Comparator Outputs (CA#) have a 953 ohm pick-off. The scope should be set to 50 ohm termination with an attenuation factor of 20.

Figure 5: Chan#0 Driver Mode and Chan#1 Compare Only Block Diagram

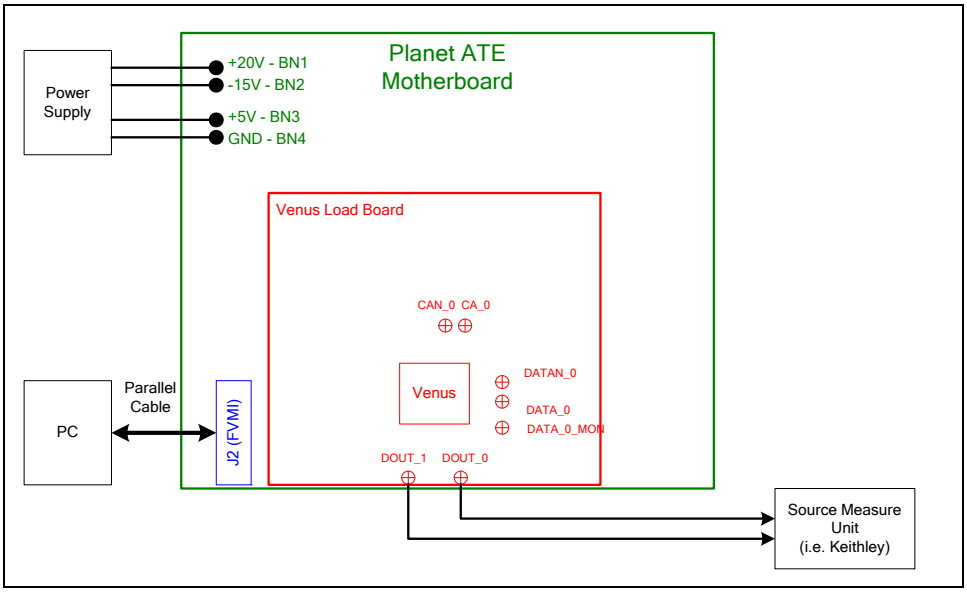


2.3.5 PMU Force Voltage or Force Current Modes

Figure 6 illustrates the recommended configuration for PMU FV/FI evaluation. The external measurement unit (MU) should be configured in the opposite mode as Venus. After the configuration is completed, use the **PMU FV/FI Levels** dialog box the change the Venus output levels.

Venus	MU
FVMI	FIMV
FIMV	FVMI

Figure 6: PMU FV/FI Block Diagram

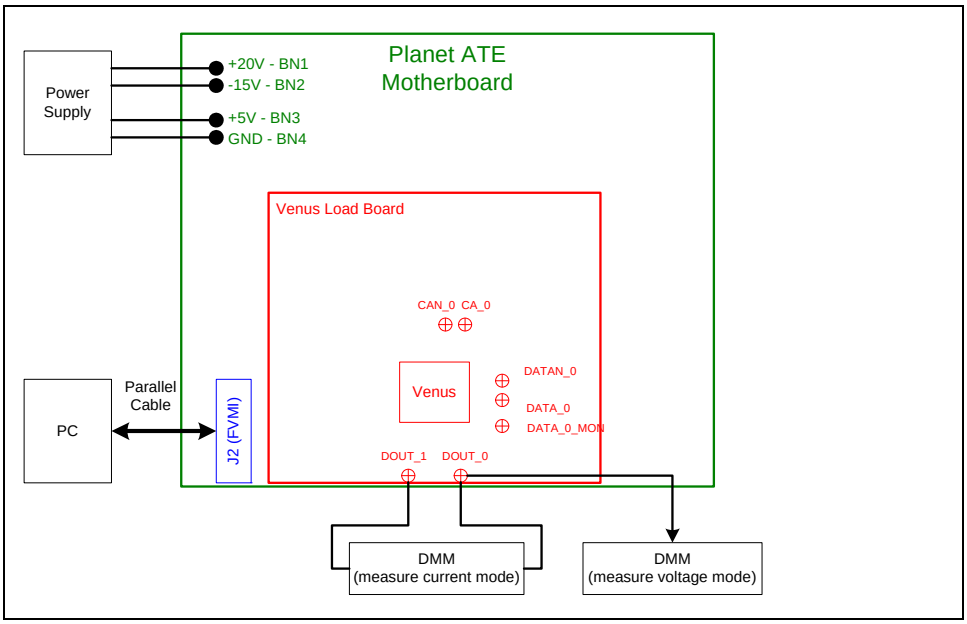


2.3.6 PMU Chan#0 in FV and Chan#1 in FI

Figure 6 illustrates the configuration for PMU Chan #0 FV and Chan #1 FI evaluation. The other channel is used to provide a proper load (current load or voltage load depending on which channel is being evaluated). This option is useful when the customer doesn't have an external measurement unit. Instead, the customer can use two DMMs to evaluate the Venus PMU.

DMM Mode	Connection
Measure Voltage	Use a 'T' connector to monitor DOUT_0 relative to GND
Measure Current	Connect in series between DOUT_0 and DOUT_1

Figure 7: PMU Chan# 0 FV and Chan #1 FI Block Diagram



2.3.7 Real Time PMU SV & Driver DVL using EN or SV Inputs

Figure 8 illustrates the configuration that uses the EN input to toggle the DOUT output between PMU FV (SV) and Driver DVL. In this application, the PMU FV is used to create the Super Voltage (SV) output. The PMU FV can output up to the VCC_SV (13V) supply minus headroom while the Driver uses the VCC (8V) supply.

The Driver is set to Real-Time Enable with CPU-DATA=0 (DVL); DVL is set to 0V. The PMU is set to Real-Time using the inverted Enable signal. The PMU is set to 12V in VR2, IR7 (32mA), and Tight feedback. The 32mA is chosen since that has the fastest response time. The PMU needs to be in Tight loopback to prevent the PMU from going into open loop when the SV switch is open.

EN Input	Driver State	SV Switch	DOUT Output
1	Enabled	Open	DVL (0V)
0	Disabled	Closed	FV (12V)

- Channel #0: Short E5 & E6 (on Motherboard) between Pin 2-3 (towards front of board)
- Channel #0: Connect differential pair to EN_0 & ENN_0 SMA connectors (on Motherboard)

Transitioning from DVL to FV (SV) requires about 100nS. Therefore the pulse generator should be set accordingly.

Real Time SV Option

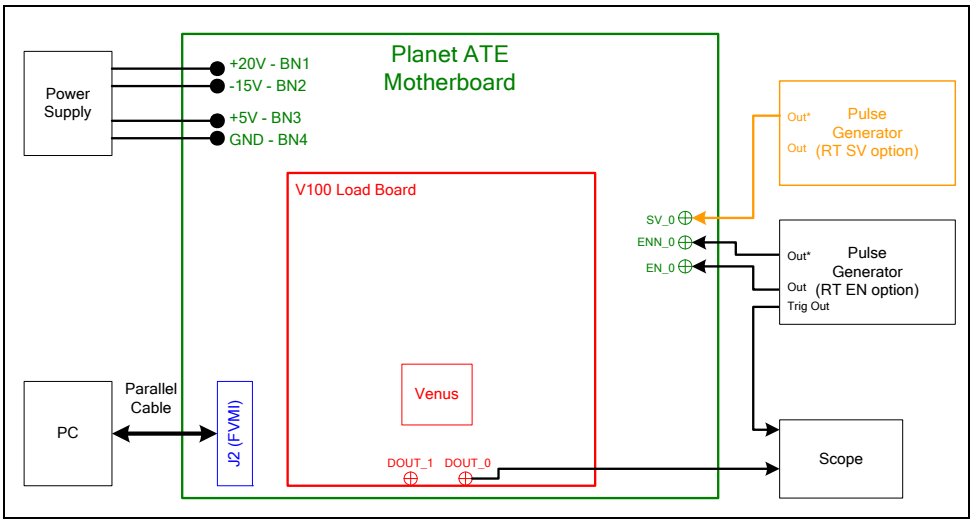
To optionally use the Real Time SV input to toggle between PMU FV (SV) and HiZ:

- Start with the Real Time SV / DVL using Enable setup
- Set **Sel-SV-EN = SV** in the ***Venus->Channel 0->Driver Path Config*** dialog box
- Channel #0: Short E7 (on Motherboard) between Pin 2-3 (towards front of board)
- Channel #0: Connect pulse generator to SV_0 SMA connector (on Motherboard)
- The Driver must be disabled. Either set the EN inputs to a static low or set **Sel-RT-EN = CPU EN** and set **CPU-EN Value = Low**.

SV Input	SV Switch	DOUT Output
0	Open	HiZ
1	Closed	FV (12V)

Note: DOUT should be connected to a Rload so DOUT gets pulled to GND when DOUT is in HiZ.

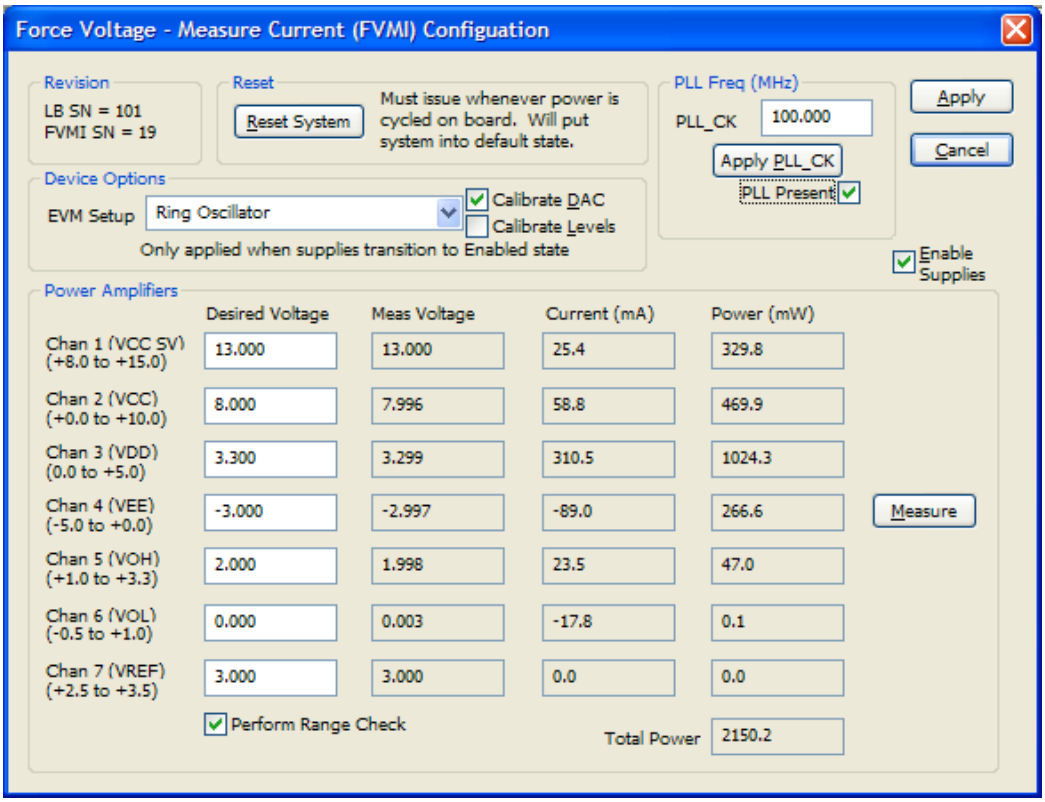
Figure 8: Toggle PMU FV (SV) and Driver DVL Block Diagram



2.4 Quick Start Instructions

1. Disable external power supply
2. Connect the power supplies cables (not provided) from the power supply to the Elevate Semiconductor EVM Motherboard.
3. Connect the parallel cable (provided) from the PC to J2 on the Octal FVMI board.
4. Setup the EVM and equipment based on the desired **EVM Setup**, see Section 2.
5. Set external power supply voltages and current limits.
6. Enable external power supply
7. Run the Elevate Semiconductor ATE GUI software; refer to Section 1.3.4 for details.
8. At the Force Voltage – Measure Current dialog box (refer to Figure 9 below):
    a. Select the **EVM Setup** option based on the setup.
    b. Select the **Enable Supplies** check box
    c. Hit the **Apply** button to power up the Venus device.
    d. If the **Calibrate DAC** is set, the software will still calibrate the DAC. The DAC is calibrated using the VFV Test&Cal mux via the MONITOR pin.
    e. If the **Calibrate Levels** is set, the software will prompt the user to disconnect the DOUT outputs before calibrating all of the Venus levels using the Ext Sense and/or Test&Cal via MONITOR. The calibration will take several minutes.
    f. The software will also measure the current consumption. Figure 9 illustrates the expected current readings.
9. The software will automatically load a default register setting into the EVM device based on the **EVM Setup** option. At this point, the Venus product should be outputting the desired signal.

Figure 9: Expected Current Readings



The **Reset System** will put the EVM and Venus device into the default state. The **Reset System** should be issued whenever the power supply is powered OFF then ON. The **Reset System** is automatically performed when the program is initially launched.

2.5 Motherboard Jumper Definition

Table 3 lists the Motherboard Jumper definitions for the Venus EVM.

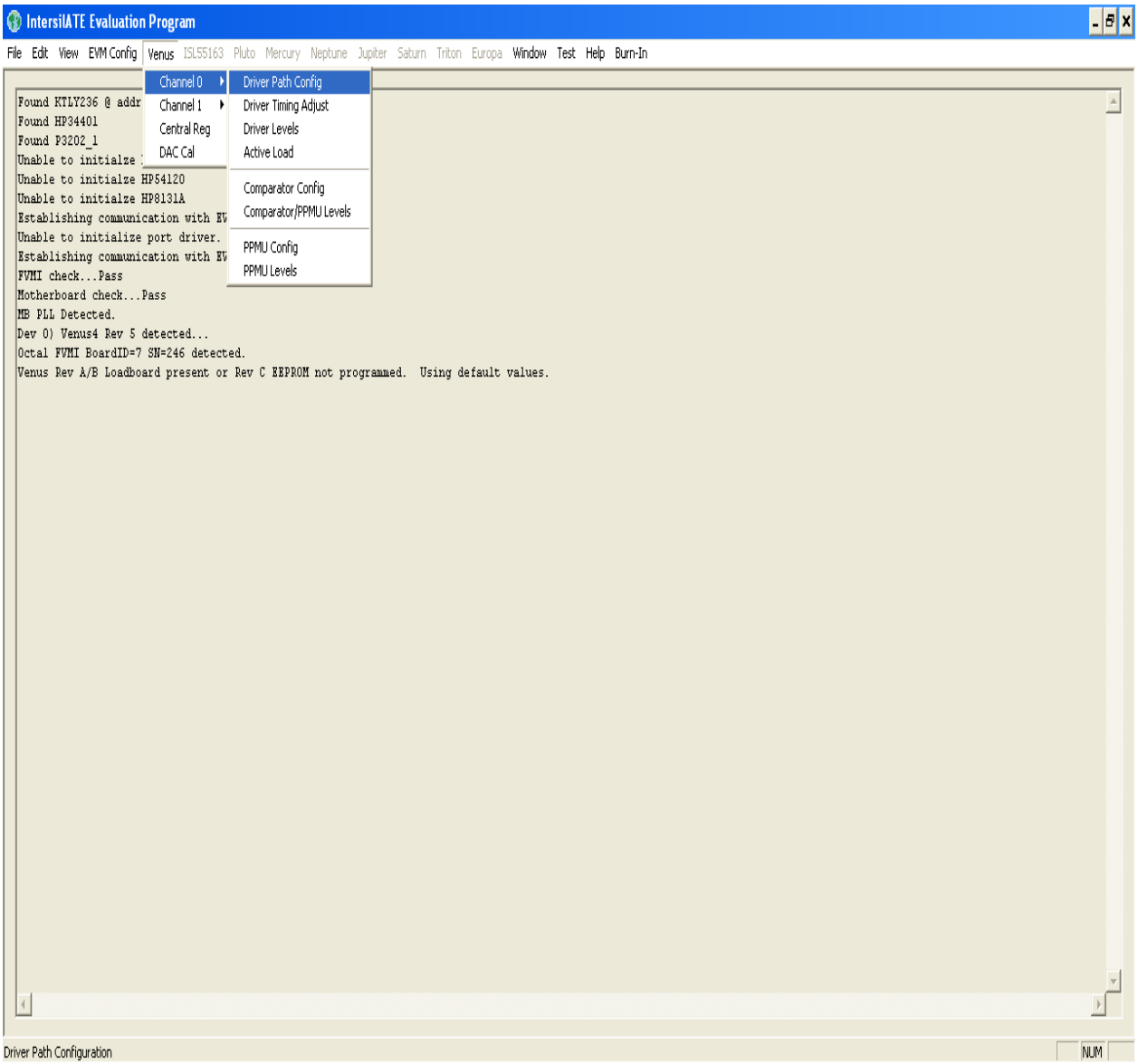
Table 3: Motherboard Jumper Definitions

TC#	Jumper	Venus	Configuration
TC_30	E12	PLL_CK	Short Pin 1 & 2. Source from Motherboard PLL Generator Short Pin 2 & 3. Source from SMA. Towards front of board. (Use for Setting for ISL55163)
TC_29	E11	PLL_CKB	Short Pin 1 & 2. Source from Motherboard PLL Generator Short Pin 2 & 3. Source from SMA. Towards front of board. (Use for Setting for ISL55163)
TC_28	E14	EXT_FORCE	Short Pin 2 & 3. Towards front of board
TC_27	E15	EXT_SENSE	Short Pin 2 & 3. Towards front of board
TC_26	E2	SV1	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_25	E10	ENN_1	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_24	E9	EN_1	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_23	E8	N/A (DATAN_1)	Short Pin 1 & 2. Do not use SMA. Use SMAs on Loadboard
TC_22	E7	N/A (DATA_1)	Short Pin 1 & 2. Do not use SMA. Use SMAs on Loadboard
TC_21	E1	SV0	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_20	E6	ENN_0	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_19	E5	EN_0	Short Pin 1 & 2. Source from latch Short Pin 2 & 3. Source from SMA
TC_18	E4	N/A (DATAN_0)	Short Pin 1 & 2. Do not use SMA. Use SMAs on Loadboard
TC_17	E3	N/A (DATA_0)	Short Pin 1 & 2. Do not use SMA. Use SMAs on Loadboard
TC_16	E13	CAP_PLL	Open
TC_15	E20	DUT_GND	Open (can optionally use SMA as DUT_GND voltage input)

2.6 Venus Menu Dialog Boxes

Figure 10 illustrates the Venus menu options. These provide access to the Venus registers.

Figure 10: Device Config Menu Options



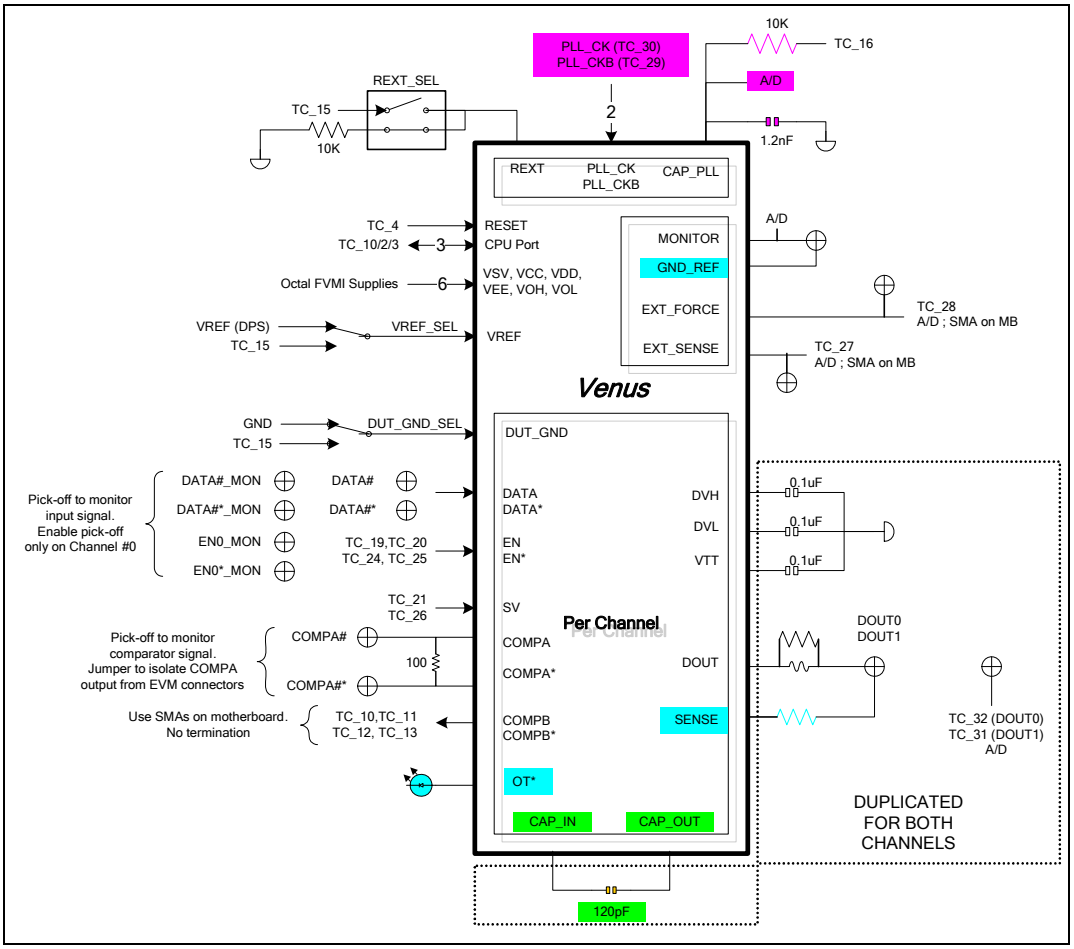
3 Venus Loadboard Detailed Description

Figure 11 illustrates the Venus EVM loadboard. The loadboard contains the Venus device as well as the necessary circuitry to validate & characterize in the bench environment.

The loadboard supports all of the various Venus Family products.

Color	Product Supported
Black	All Venus products
Green	Venus, Venus3, ISL55162, ISL55164
Turquoise	Venus4, ISL55161, ISL55163
Pink	Installed but not used in ISL55163

Figure 11: Venus Loadboard Detailed Block Diagram



3.1 ADC and Analog Mux

The Octal FVMI contains a 24-bit ADC and analog muxes. Error! Reference source not found. lists the Venus EVM loadboard specific mux input sources.

Table 4: FVMI Analog Mux – VINPOS(A) & VINNEG(A) Mapping

Addr	VINP#	VINPOS(A)	VINN#	VINNEG(A)
7	VINP8	Reserved	VINN8	VREF Divider
8	VINP9	MONITOR	VINN9	No connect MON_REF
9	VINP10	EXT_FORCE	VINN10	No connect
10	VINP11	R_EXT	VINN11	No connect
11	VINP12	CAP_PLL	VINN12	No connect
12	VINP13	TC-31 (DOUT_1)	VINN13	No connect
13	VINP14	TC-32 (DOUT_0)	VINN14	EXT_SENSE

3.2 Venus Loadboard Controller

The Venus loadboard contains one 8-bit latch (register) and a 16K EEPROM. The control signals originate from the motherboard. The C-Bits originate from the Octal FVMI board.

Table 5: Loadboard C-Bit (J6) Signal Definitions

CBIT#	Def	Bit Name	Bit Description
6:1	0	CBIT[6:1]	Unused
7	0	LATCH_CS	U3 Latch CS
8	-	Reserved	Used by ATE test board
9	-	Reserved	Used by Octal FVMI board

Table 6: Venus Loadboard Latches (U3) Signal Definitions

Bit #	Bit Name	Bit Description
1:0	REXT_SEL	0=Connect REXT to 10K. (default) 1=Connect REXT to TC15 (for continuity/leakge test)
3:2	DG0_SEL	0=Connect DUT_GND#0 to GND (default) 1=Connect DUT_GND#0 to TC15 (for continuity/leakge test)
5:4	DG1_SEL	0=Connect DUT_GND#1 to GND (default) 1=Connect DUT_GND#1 to TC15 (for continuity/leakge test)
7:6	VREF_SEL	0=Connect VREF pin to VREF DUT supply (default) 1=Connect VREF pin to TC15 (for continuity/leakge test)

4 Layout Considerations

This section provides some layout guidelines. Customers may employ different layout strategies to achieve the desired performance.

4.1 Conjugate Termination

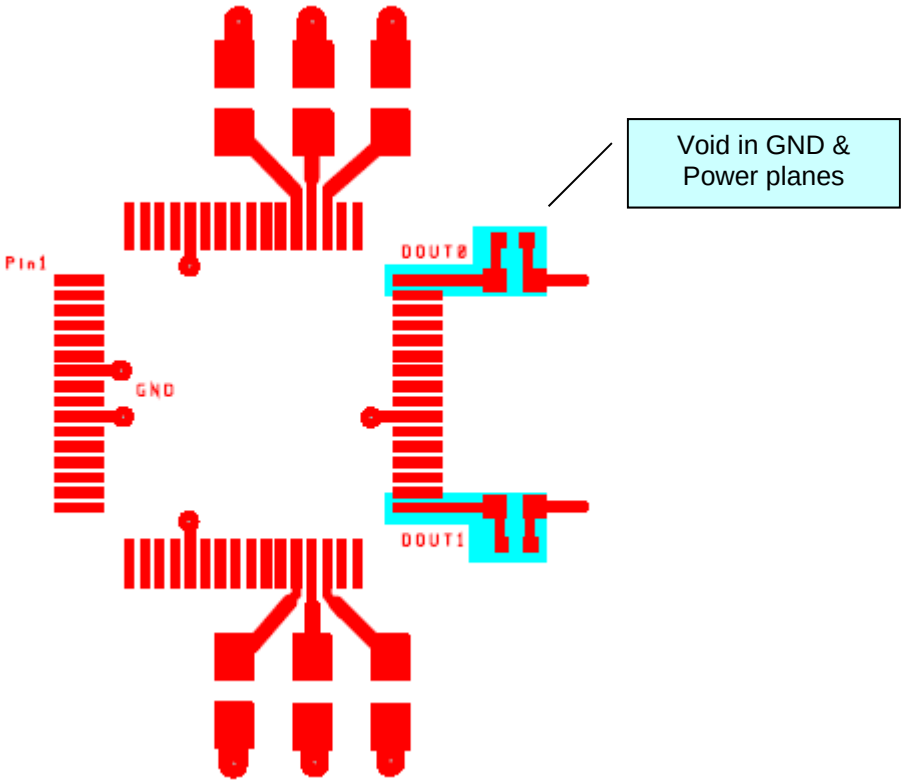
The Inductor | Resistor conjugate termination is used to compensate for the lumped capacitance from Venus's Driver output and pads.

- should be placed as close to the DOUT pad as possible
- Use 0402 Resistor component size
- Use 0603 Inductor component size. Inductor should have low R. In addition to AC performance, need to minimize the R for when doing parametric (PMU) measurements. The Inductor should be able to tolerate large DC currents; up to 32mA in normal operating modes and possible 100mA in a short circuit condition.
- Create a 'void' in the GND plane beneath the DOUT pad and Inductor/Resistor components

4.2 CAP DVH/DVL/VTT

The DVH/DVL/VTT capacitors are used to provide the Driver AC current.

- should be placed as close to the pad as possible
- match trace lengths as close as possible; including Channel to Channel to obtain symmetric performance
- The EVM uses 0805 components for ease in troubleshooting. Customers can use 0603 or capacitor packs.



5 Document Revision History

Revision	Date	Description
A01	9/18/03	Initial Draft. Extracted from Venus EVM User's Guide.
A02	11/7/03	Added LVDS Output configuration option, section 2.3.3
C01	1/27/05	Updated Section 2 for Motherboard Rev C and Loadboard Rev C support • Motherboard Rev A/B and Loadboard Rev B are no longer described in this document. Added Detailed Block Diagram, see Section 3 Added Controller Logic block diagram, see Section 3.1
D01	5/26/2005	Rev D and Rev D2 support
D02	2/20/2007	Overhauled Section 2.3.4. Now call it Drive Only and Compare Only Added Real Time SV/DVL, Section 2.3.7
G01	6/11/2011	Added ISL55161/2/3/4 Products to document.